BASIC OF ELECTRONICS

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Field-Effect Transistor (FET)

- **4.4 MOSFET Operation and Construction**
  - *4.4.1 Depletion MOSFET*
  - *4.4.2 Enhancement MOSFET*
- **4.5 Biasing of FETs**
- **4.6 Analysis of a CS Amplifier**
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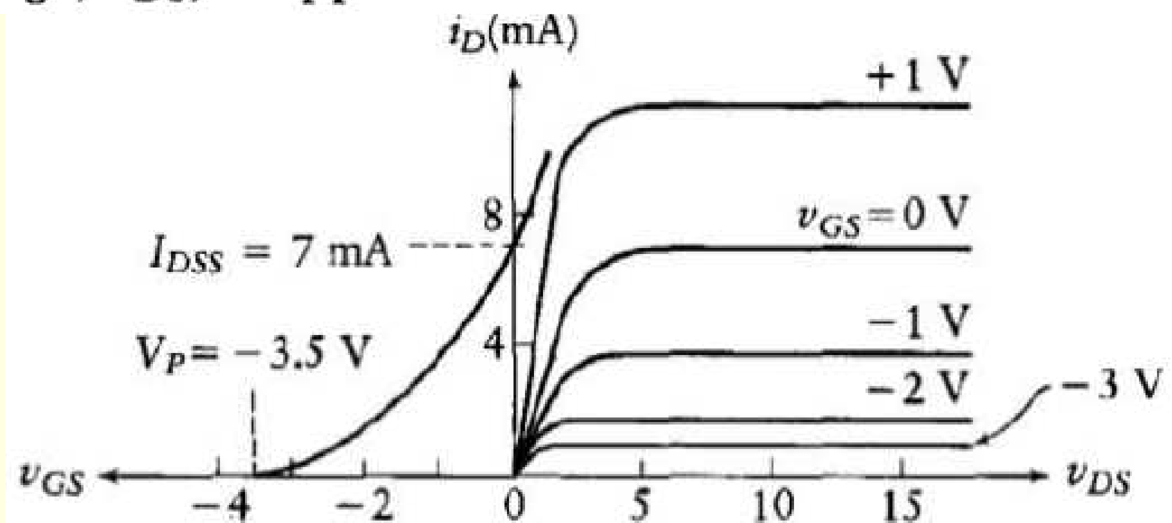
4.4 MOSFET Operation and Construction

In this section, we consider the metal-oxide-semiconductor FET (MOSFET). This FET is constructed with the gate terminal insulated from the channel with a silicon dioxide (SiO_2) dielectric and is constructed in either a *depletion* or an *enhancement* mode. We define and consider these two types in the next sections.

4.4 MOSFET Operation and Construction

Depletion MOSFET

The constructions of the *n*-channel and the *p*-channel depletion MOSFET are shown in Figures 4.9 and 4.10, respectively. Each of these figures shows the construction, the symbol, the transfer characteristic, and the i_D-v_{GS} characteristics. The depletion MOSFET is constructed (as shown in Figure 4.9(a) for the *n*-channel and Figure 4.10(a) for the *p*-channel) with a physical channel constructed between the drain and the source. As a result, i_D exists between drain and source when a voltage, v_{DS}, is applied.



(c) Transfer and i_D-v_{GS} characteristics

The *n*-channel depletion MOSFET.

4.4 MOSFET Operation and Construction

Depletion MOSFET

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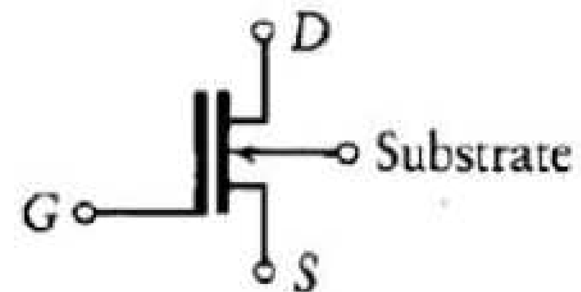
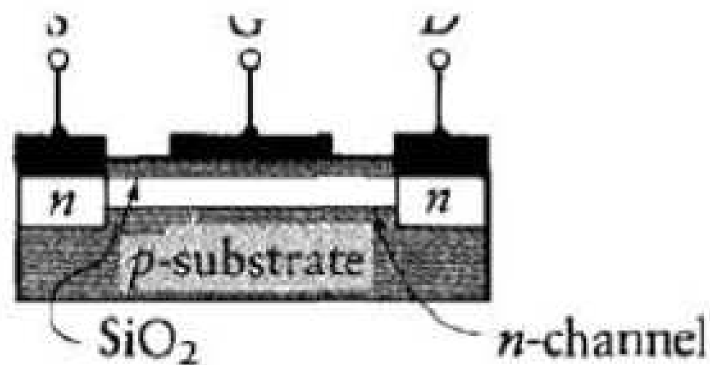


(b) Symbol

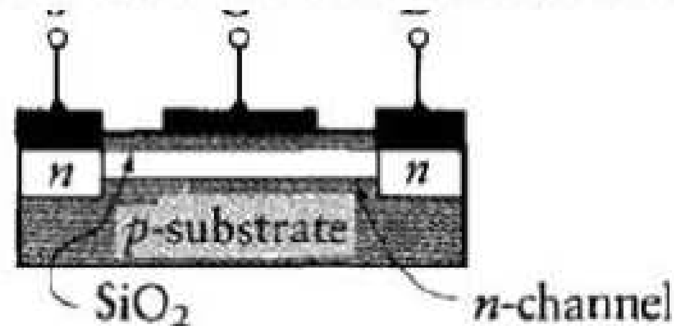


(a) Schematic of physical structure

The *n*-channel depletion MOSFET.

4.4 MOSFET Operation and Construction

The n-channel depletion MOSFET of Figure 4.9 is established on a p-substrate, which is a p-doped silicon. The n-doped source and drain wells form low-resistance connections between the ends of the n-channel and the aluminimum contacts of the source (S) and the drain (D). An SiO_2 layer, which is an insulator, is grown on the top surface of the n-channel, as shown in Figure 4.9(a). An aluminum pad is deposited on the SiO_2 insulator to form the gate (G) terminal. The performance of the depletion MOSFET, as can be seen from Figures 4.9(c) and 4.10(c), is similar to that of the JFET. The JFET is controlled by the pn junction between the gate and the drain end of the channel. No such junction exists in the enhancement MOSFET, and the SiO_2 layer acts as the insulator. For the n-channel MOSFET, shown in Figure 4.9, a negative v_{GS} will push the electrons out of the channel region, hence depleting the channel.

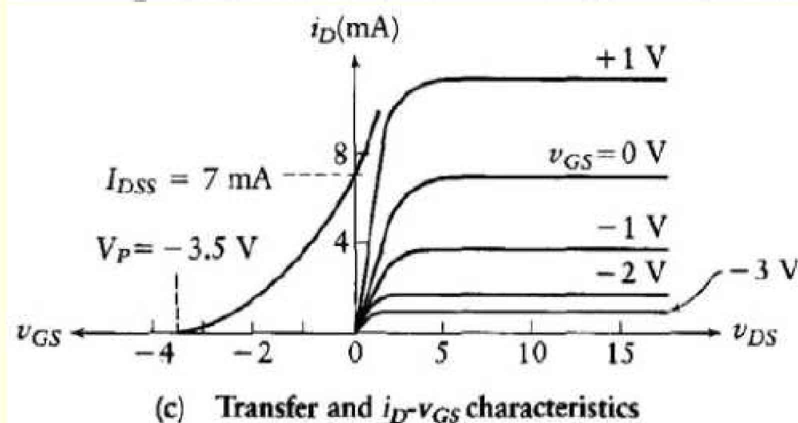


(a) Schematic of physical structure

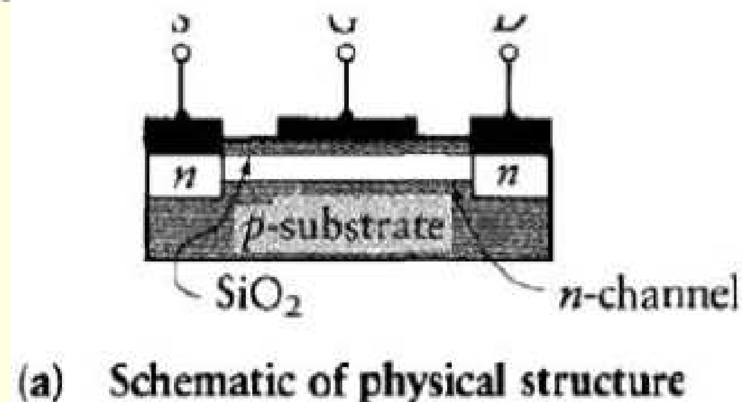
The n-channel depletion MOSFET.

4.4 MOSFET Operation and Construction

The *n*-channel depletion MOSFET of Figure 4.9 is established on a *p*-substrate, which is a *p*-doped silicon. The *n*-doped source and drain wells form low-resistance connections between the ends of the *n*-channel and the aluminimum contacts of the source (*S*) and the drain (*D*). An SiO_2 layer, which is an insulator, is grown on the top surface of the *n*-channel, as shown in Figure 4.9(a). An aluminum pad is deposited on the SiO_2 insulator to form the gate (G) terminal. The performance of the depletion MOSFET, as can be seen from Figures 4.9(c) and 4.10(c), is similar to that of the JFET. The JFET is controlled by the *pn* junction between the gate and the drain end of the channel. No such junction exists in the enhancement MOSFET, and the SiO_2 layer acts as the insulator. For the *n*-channel MOSFET, shown in Figure 4.9, a negative v_{GS} will push the electrons out of the channel region, hence depleting the channel.



(c) Transfer and i_D-v_{GS} characteristics

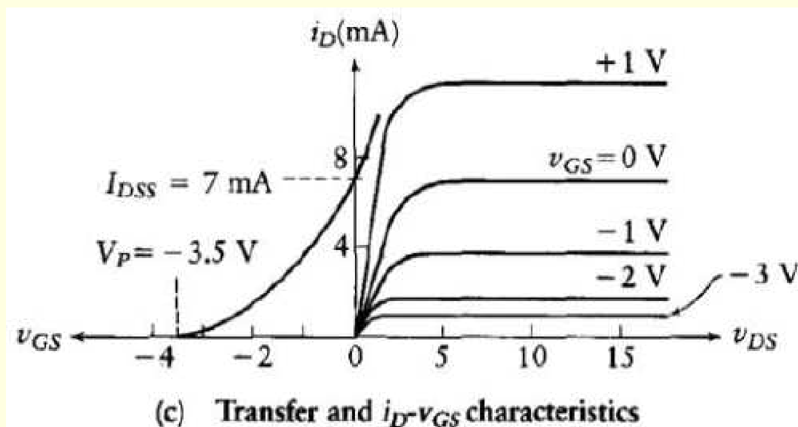


(a) Schematic of physical structure

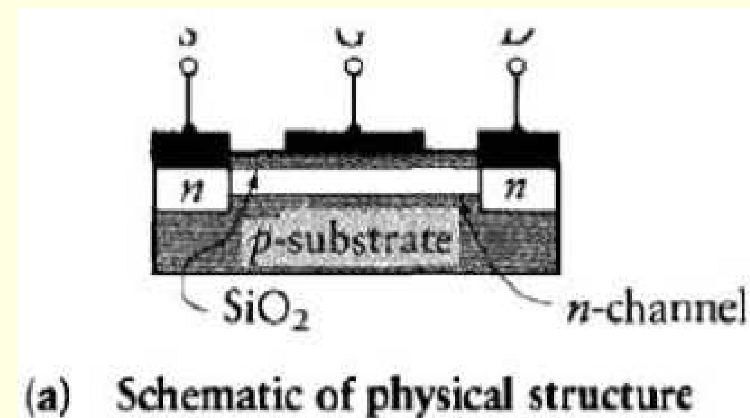
4.4 MOSFET Operation and Construction

When v_{GS} reaches V_p, the channel will be pinched off. Positive values of v_{GS} increase channel size, resulting in an increase of drain current. This is indicated on the characteristic curves of Figure 4.9(c).

Notice that the depletion MOSFET can operate with either positive or negative values of v_{GS}. We can use the same Shockley equation (equation (4.1)) to approximate the curves for negative v_{GS}. Notice, however, that the transfer characteristic continues on for positive values of v_{GS}. Since the gate is insulated from the channel, the gate current is negligibly small (10^{-12} A), and v_{GS} can be of either polarity.



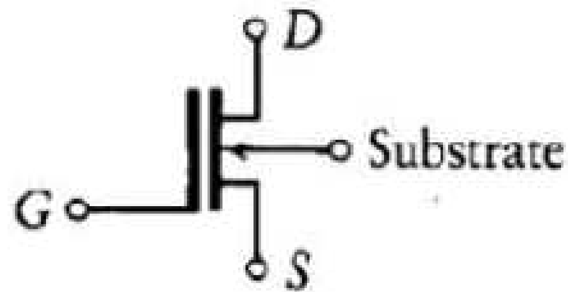
(c) Transfer and i_D-v_{GS} characteristics



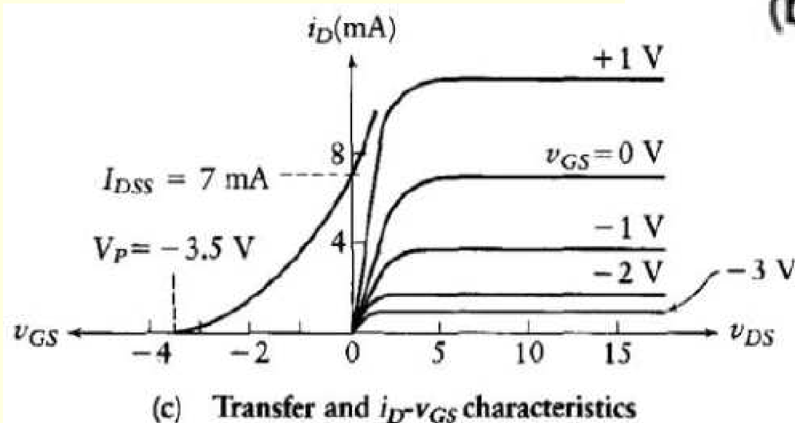
(a) Schematic of physical structure

4.4 MOSFET Operation and Construction

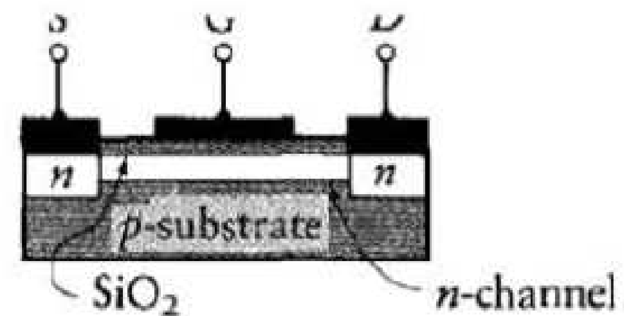
As we can see from Figures 4.9(b) and 4.10(b), the symbol for the MOSFET has a fourth terminal, the *substrate*. The arrowhead points in for an *n*-channel and out for a *p*-channel. The *p*-channel depletion MOSFET, which is shown in Figure 4.10, is the same as Figure 4.9, except we reverse the *n*- and *p*-materials and reverse the polarity of the voltages and currents.



(b) Symbol



(c) Transfer and i_D-v_{GS} characteristics

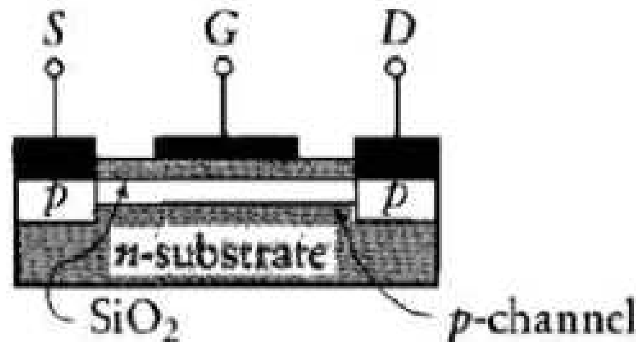


(a) Schematic of physical structure

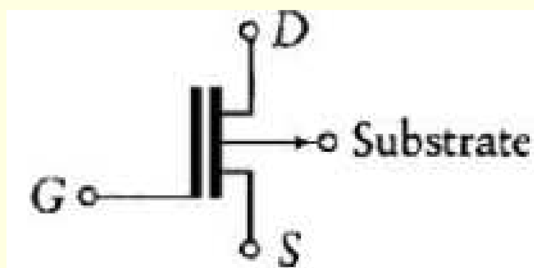
4.4 MOSFET Operation and Construction

As we can see from Figures 4.9(b) and 4.10(b), the symbol for the MOSFET has a fourth terminal, the *substrate*. The arrowhead points in for an *n*-channel and out for a *p*-channel. The *p*-channel depletion MOSFET, which is shown in Figure 4.10, is the same as Figure 4.9, except we reverse the *n*- and *p*-materials and reverse the polarity of the voltages and currents.

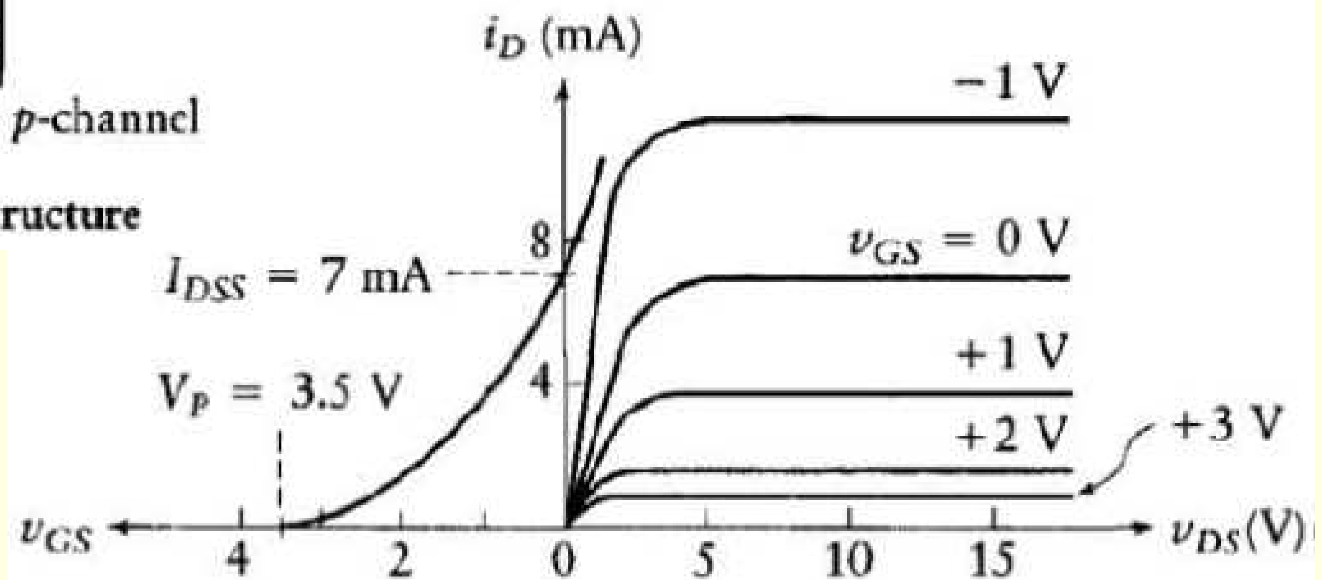
The *p*-channel depletion MOSFET.



(a) Schematic of physical structure



(b) Symbol



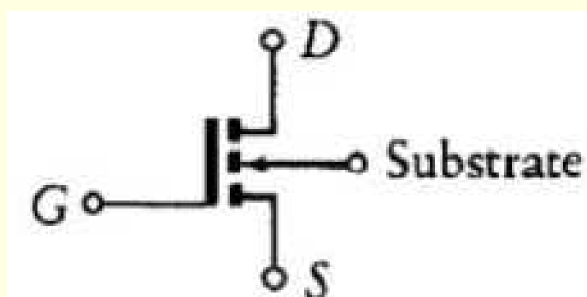
(c) Transfer and i_D-v_{GS} characteristics

4.4 MOSFET Operation and Construction

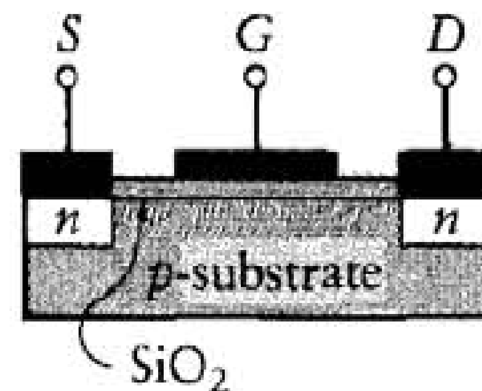
Enhancement MOSFET

The enhancement MOSFET is shown in Figure 4.11. It differs from the depletion MOSFET in that it does not have the thin *n*-layer but requires a positive voltage between the gate and source to establish a channel. This channel is formed by the action of a positive gate-to-source voltage, v_{GS}, which attracts electrons from the substrate region between the *n*-doped drain and source. Positive v_{GS} causes electrons to accumulate at the surface beneath the oxide layer. When the voltage reaches a threshold value, V_T, enough electrons are attracted to this region to make it act like a conducting *n*-channel. No appreciable current i_D will exist until v_{GS} exceeds V_T.

The *n*-channel enhancement MOSFET.



(b) Symbol



(a) Schematic of physical structure

4.4 MOSFET Operation and Construction

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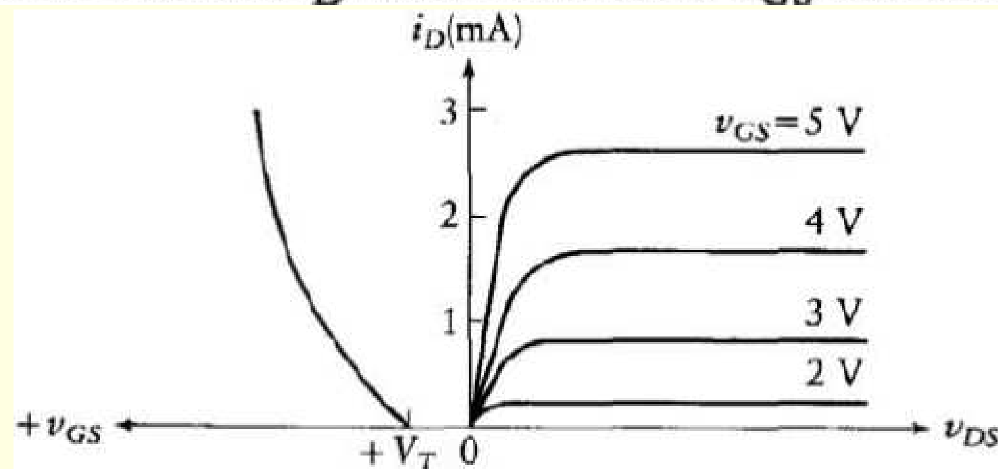
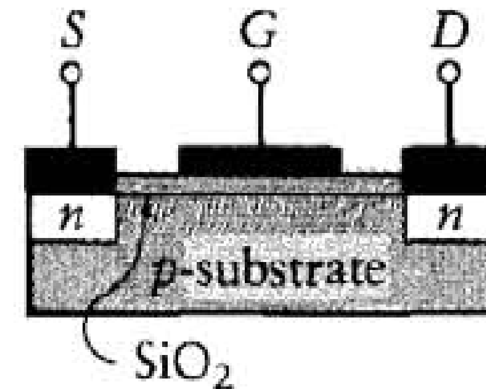


(c) Transfer and i_D-v_{DS} characteristics



(a) Schematic of physical structure

4.4 MOSFET Operation and Construction

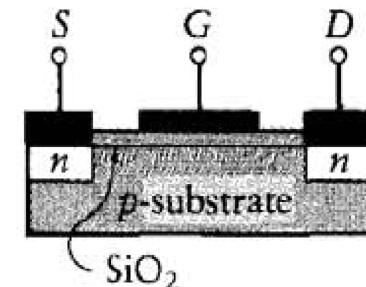
No value of I_{DSS} exists for the enhancement MOSFET, since the drain current is zero until the channel has been formed. I_{DSS} is zero at $v_{GS} = 0$. For values of

$$v_{GS} > V_T$$

the drain current in saturation can be calculated from the equation

$$i_D = k(v_{GS} - V_T)^2 \tag{4.10}$$

The value of k depends upon the construction of the MOSFET and is primarily a function of the width and length of the channel. A typical value for k is 0.3 mA/V^2, and the threshold voltage, V_T, is specified by the manufacturer. We



(a) Schematic of physical structure

The n-channel enhancement MOSFET.

4.4 MOSFET Operation and Construction

can find a value for g_m by differentiating equation (4.10), as we did with JFETs, with the result

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = 2k(v_{GS} - V_T) \tag{4.11}$$

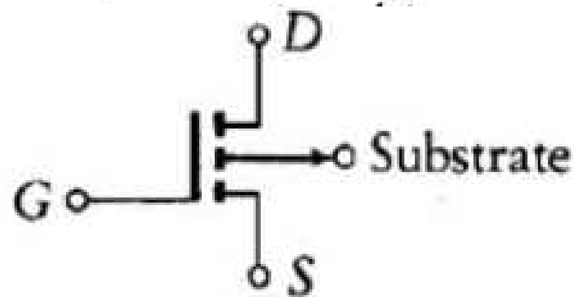
If

$$v_{GS} < V_T$$

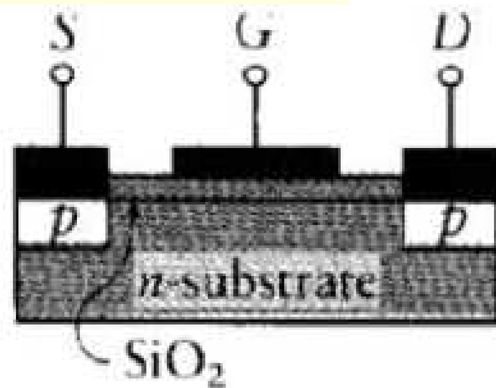
then $i_D = 0$.

4.4 MOSFET Operation and Construction

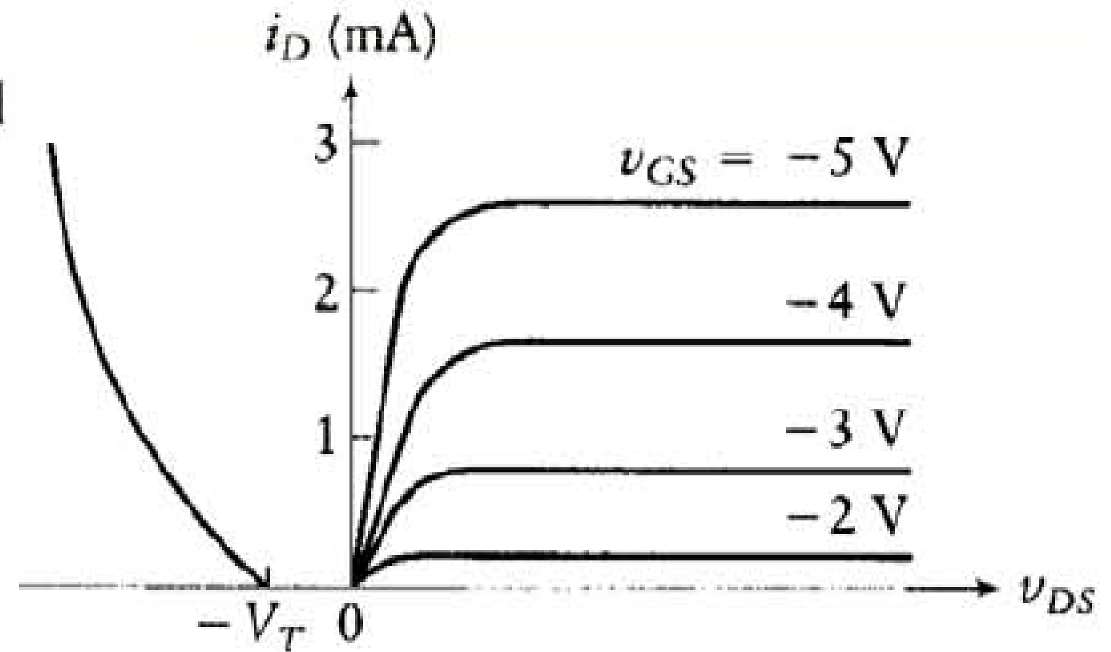
The p-channel enhancement MOSFET is shown in Figure 4.12 and, as can be seen, displays similar but opposite characteristics to those of the n-channel enhancement MOSFET.



(b) Symbol



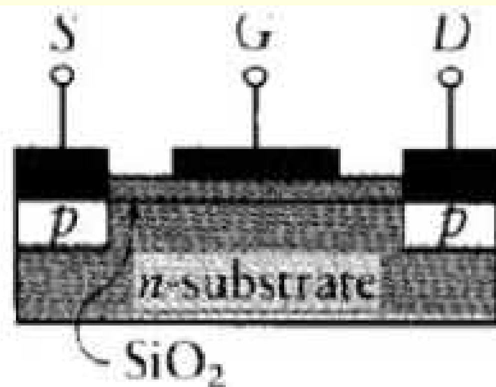
(a) Schematic of physical structure



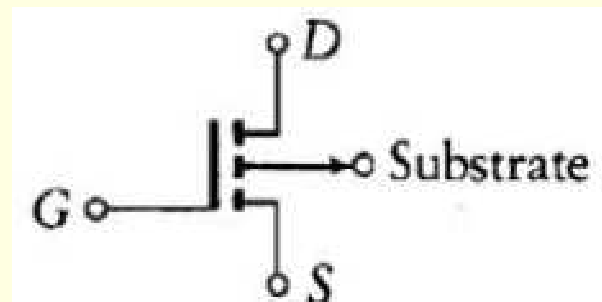
(c) Transfer and i_D-v_{GS} characteristics

4.4 MOSFET Operation and Construction

Although it is more restricted in operating range than the depletion MOSFET, the enhancement MOSFET is useful in IC applications (see Chapter 15) because of its small size and simple construction. The gate for both *n*- and *p*-channel MOSFETs is a metal deposit on a silicon-oxide layer. The construction begins with a substrate material (*p*-type for *n*-channel; *n*-type for *p*-channel) on which the opposite type of material is diffused to form the source and drain. Notice that the symbol for an enhancement MOSFET, which is shown in Figures 4.11 and 4.12, shows a broken line between source and drain to indicate that no channel initially exists.



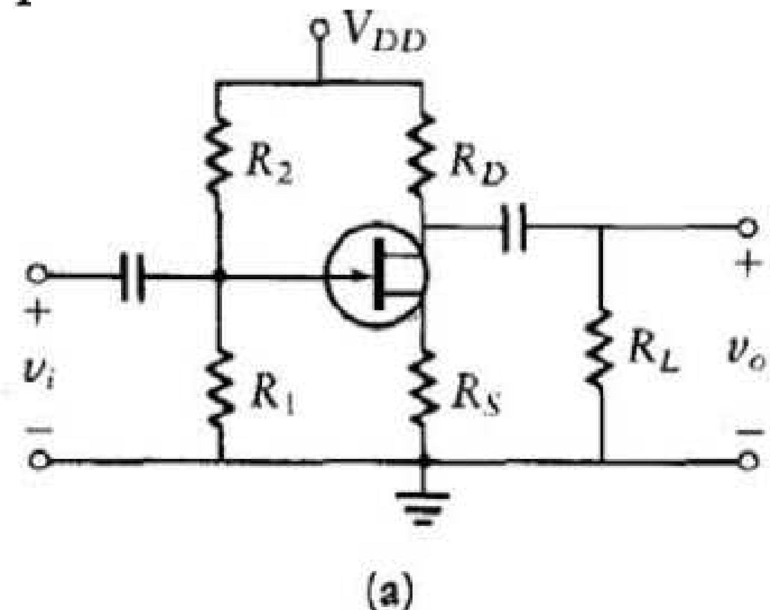
(a) Schematic of physical structure



(b) Symbol

4.5 Biasing of FETs

The same basic circuits of Figure 3.6 that are used for biasing BJTs can also be used for JFETs and depletion MOSFETS. However, for the active region of the JFET and the depletion-mode MOSFET, the polarity of v_{GS} can be opposite from that of the drain voltage source. In selecting the operating point, voltage of the opposite polarity is not available from the source to meet the requirements of the circuit. It may be necessary to delete R_2 (see Figure 4.13) so only voltage of correct polarity is acquired. It is not always possible to find resistor values to achieve a particular Q-point. In such instances, selecting a new Q-point can sometimes provide a solution to the problem.

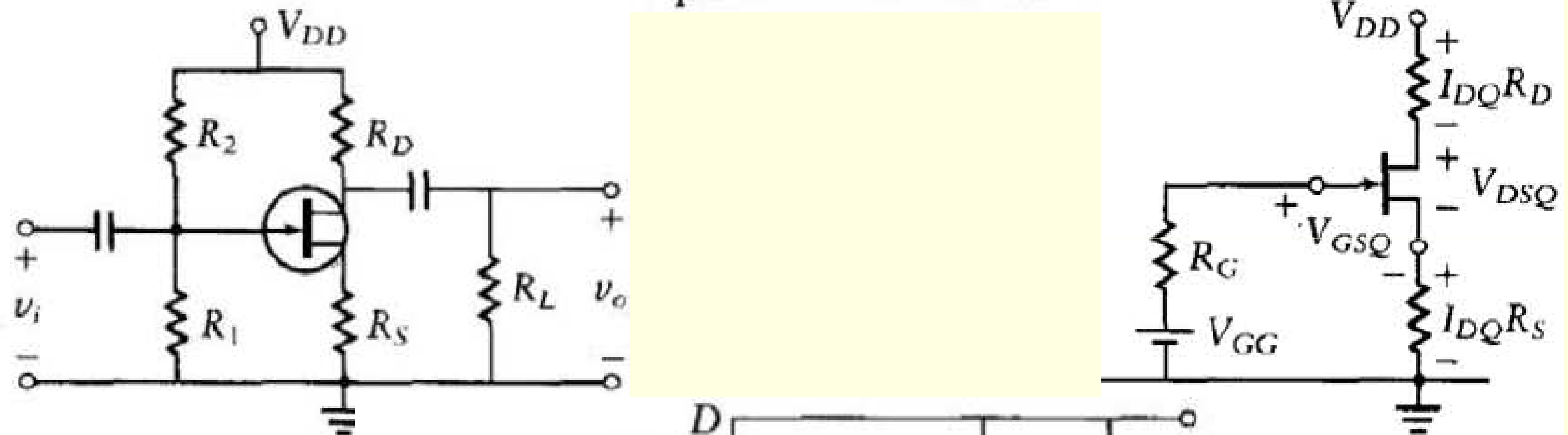


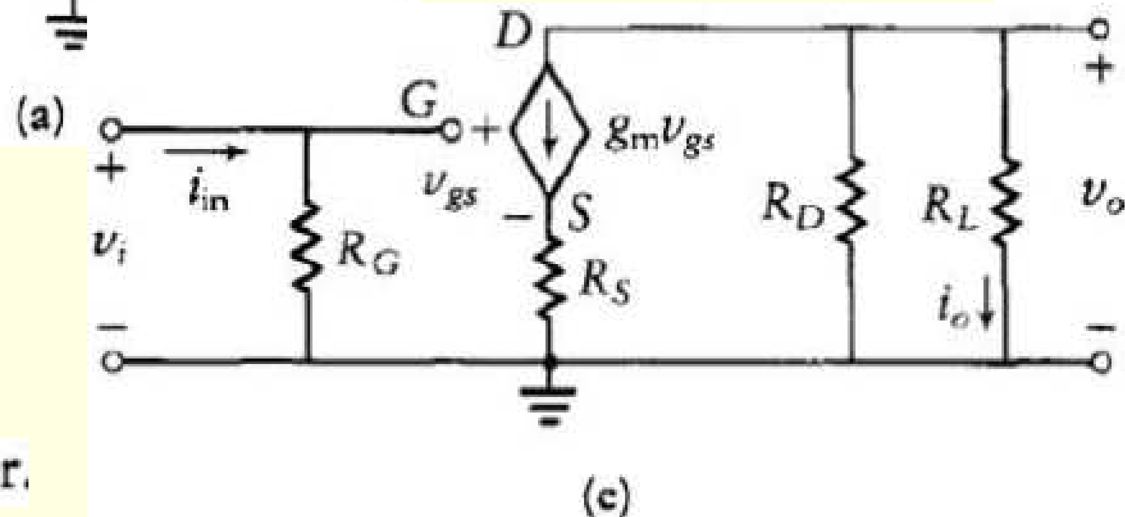
(a)

4.5 Biasing of FETs

We consider here the bias equations for the CS amplifier, shown in Figure 4.13, where we use a JFET. The bias methods are similar for depletion MOSFETs.

Figure 4.13(a) illustrates a FET amplifier using one dc voltage source for biasing. We form the Thevenin equivalent of the bias circuit to obtain





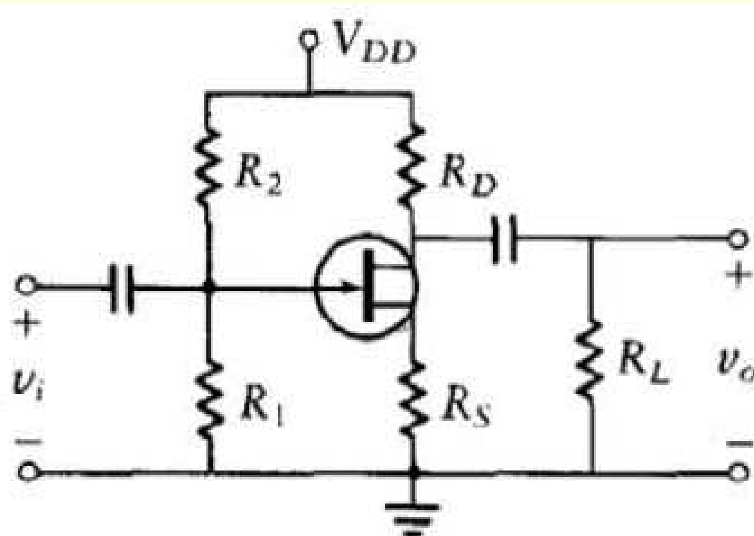
FET amplifier.

4.5 Biasing of FETs

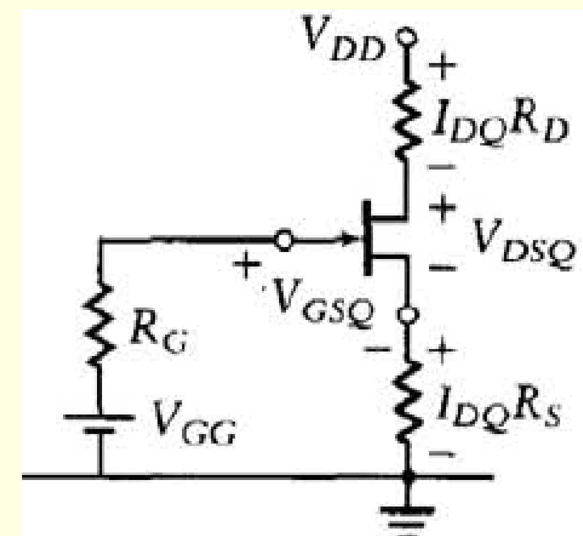
Figure 4.13(a) illustrates a FET amplifier using one dc voltage source for biasing. We form the Thevenin equivalent of the bias circuit to obtain

$$R_G = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad (4.12a)$$

$$V_{GG} = \frac{V_{DD} R_1}{R_1 + R_2} \quad (4.12b)$$



FET amplifier. (a)



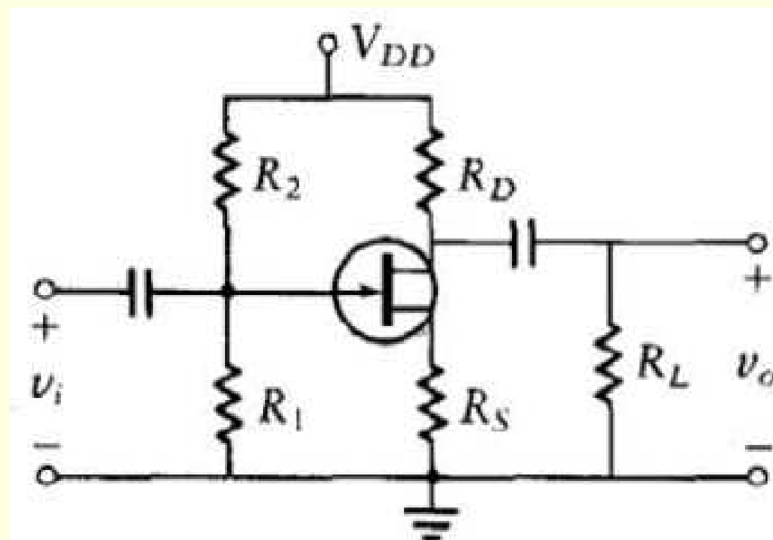
(b)

4.5 Biasing of FETs

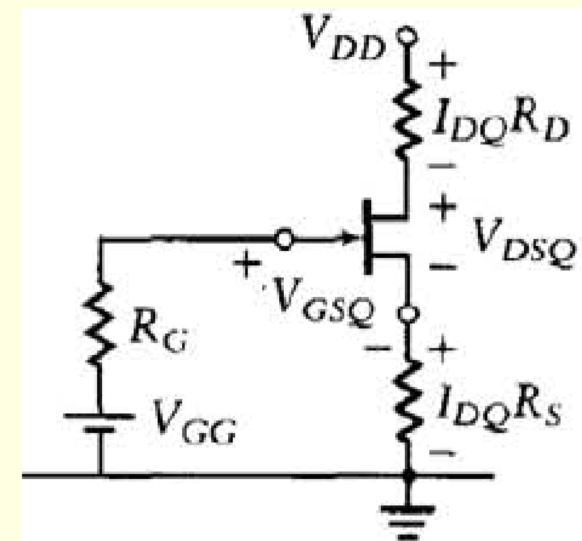
Since we have three unknown variables, I_{DQ}, V_{GSQ}, and V_{DSQ}, we need three dc equations. First, the dc equation around the gate-source loop is formed from Figure 4.13(b), as follows:

$$V_{GG} = V_{GSQ} + I_{DQ}R_S \tag{4.13}$$

Notice that since the gate current is zero, a zero voltage drop exists across R_G.



FET amplifier. (a)

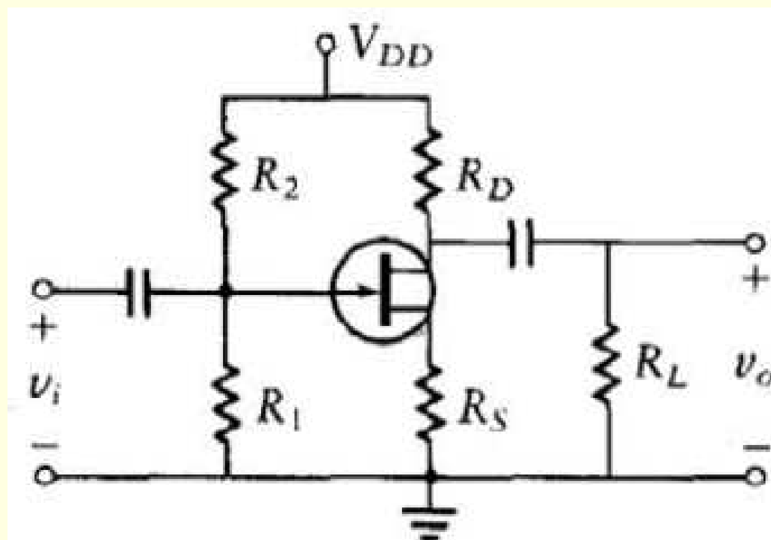


(b)

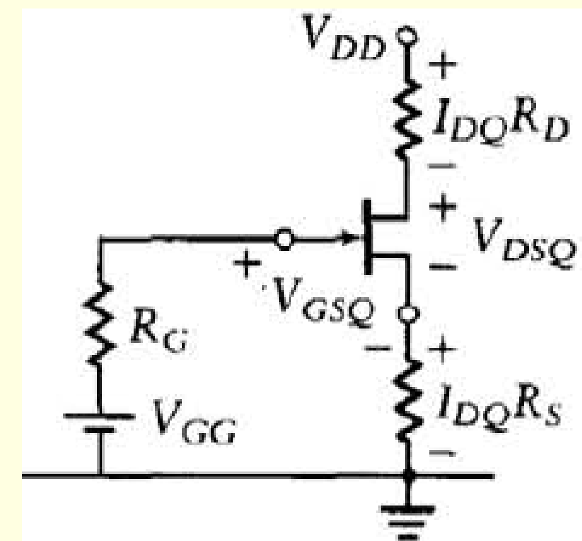
4.5 Biasing of FETs

A second dc equation is found from the Kirchhoff's law equation in the drain-source loop, as follows:

$$V_{DD} = V_{DSQ} + I_{DQ}(R_S + R_D) \tag{4.14}$$



FET amplifier. (a)

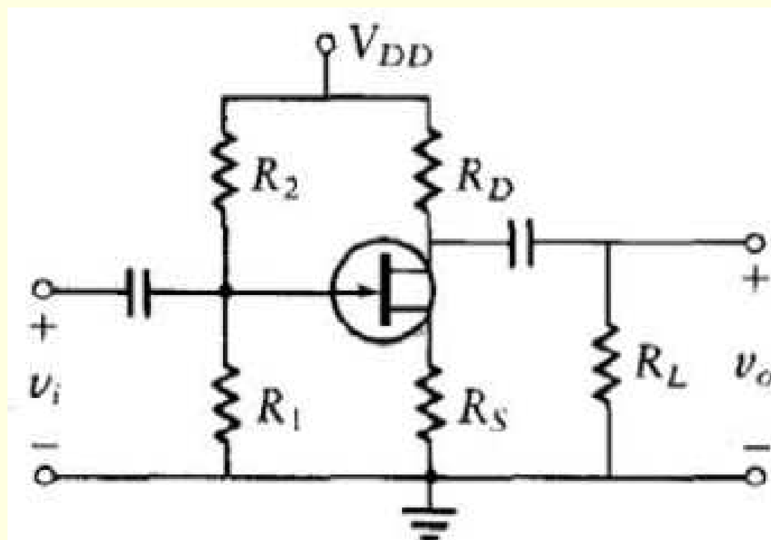


(b)

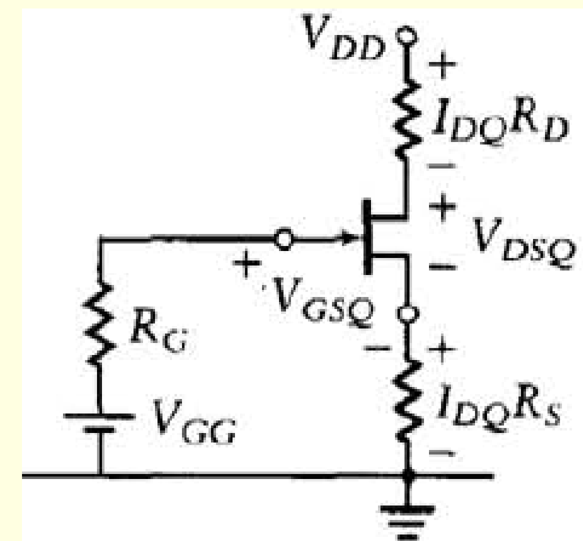
4.5 Biasing of FETs

The third dc equation necessary to establish the bias point is found from equation (4.1), which is repeated here with $i_D = I_{DQ}$ and $v_{GS} = V_{GSQ}$.

$$\frac{I_{DQ}}{I_{DSS}} = \left(1 - \frac{V_{GSQ}}{V_p}\right)^2 \tag{4.15}$$



FET amplifier. (a)

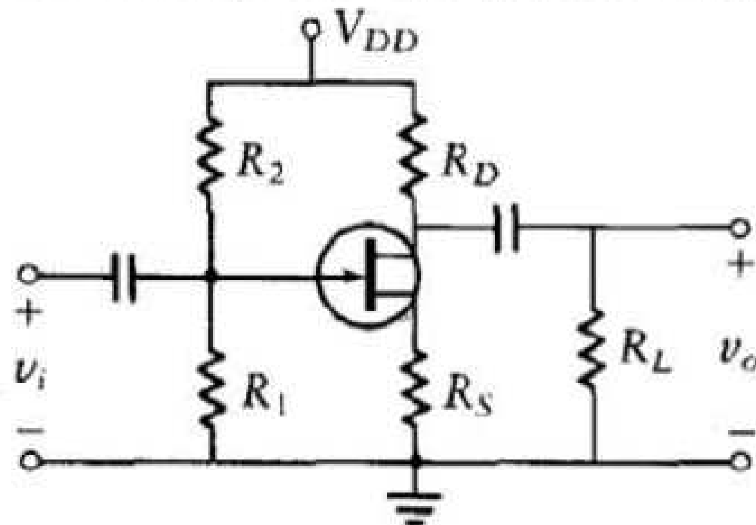


(b)

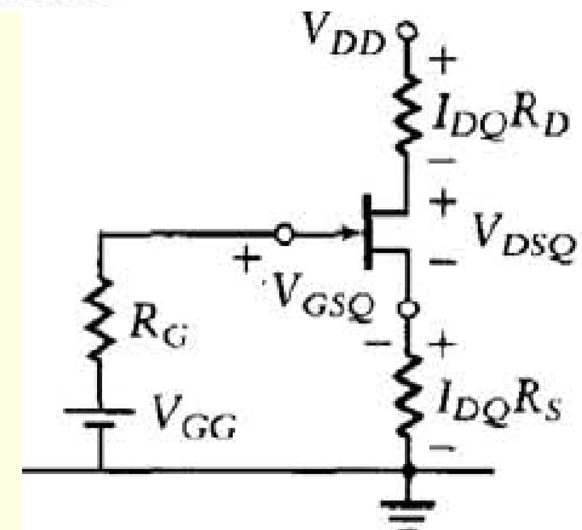
4.5 Biasing of FETs

These three equations are sufficient to establish the bias for the JFET and depletion MOSFET, which are used for linear amplifiers. The enhancement MOSFET is used for digital ICs.

Note that we do not need to put the *Q*-point in the center of the ac load line as we did for BJT biasing. This is because we normally use a FET amplifier at the input to the amplifier to take advantage of the high input resistance. At this point, the voltage levels are so small that we do not drive the amplifier with large excursions. Also, since the FET characteristic curves are nonlinear, we would produce distortion with large input excursions.



FET amplifier. (a)



(b)

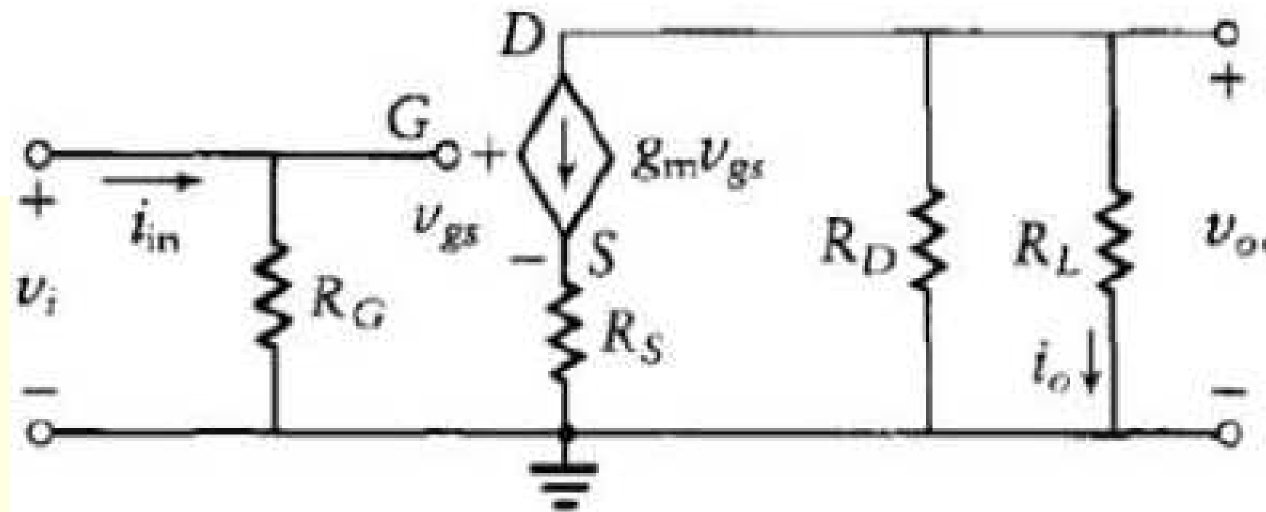
4.6 Analysis of a CS Amplifier

Figure 4.13(c) shows the ac equivalent circuit for the FET amplifier. We assume r_{DS} is large compared to $R_D \| R_L$, so it can be neglected. Writing a KVL equation around the gate circuit, we find

$$v_{gs} = v_i - R_S i_D = v_i - R_S g_m v_{gs}$$

Solving for v_{gs} yields

$$v_{gs} = \frac{v_i}{1 + R_S g_m}$$



(c)

FET amplifier.

4.6 Analysis of a CS Amplifier

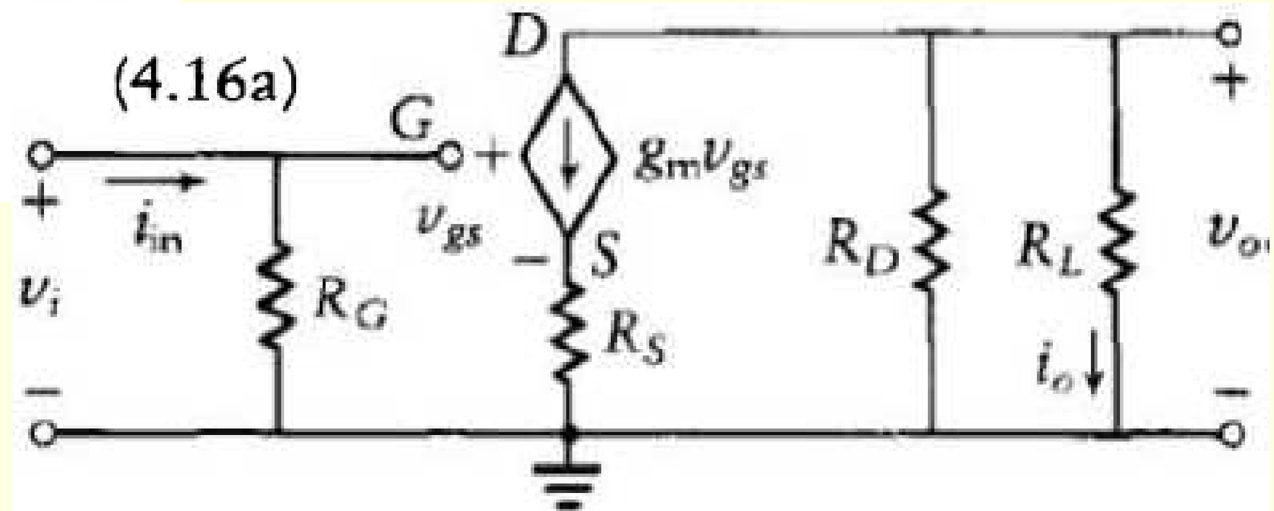
The output voltage, v_o, is given by

$$v_o = -i_d(R_D \parallel R_L) = \frac{-(R_D \parallel R_L)g_m v_i}{1 + R_S g_m}$$

The voltage gain, A_v, is

$$A_v = \frac{v_o}{v_i} = \frac{-g_m(R_D \parallel R_L)}{1 + R_S g_m}$$

$$= \frac{-(R_D \parallel R_L)}{R_S + 1/g_m} \qquad (4.16a)$$



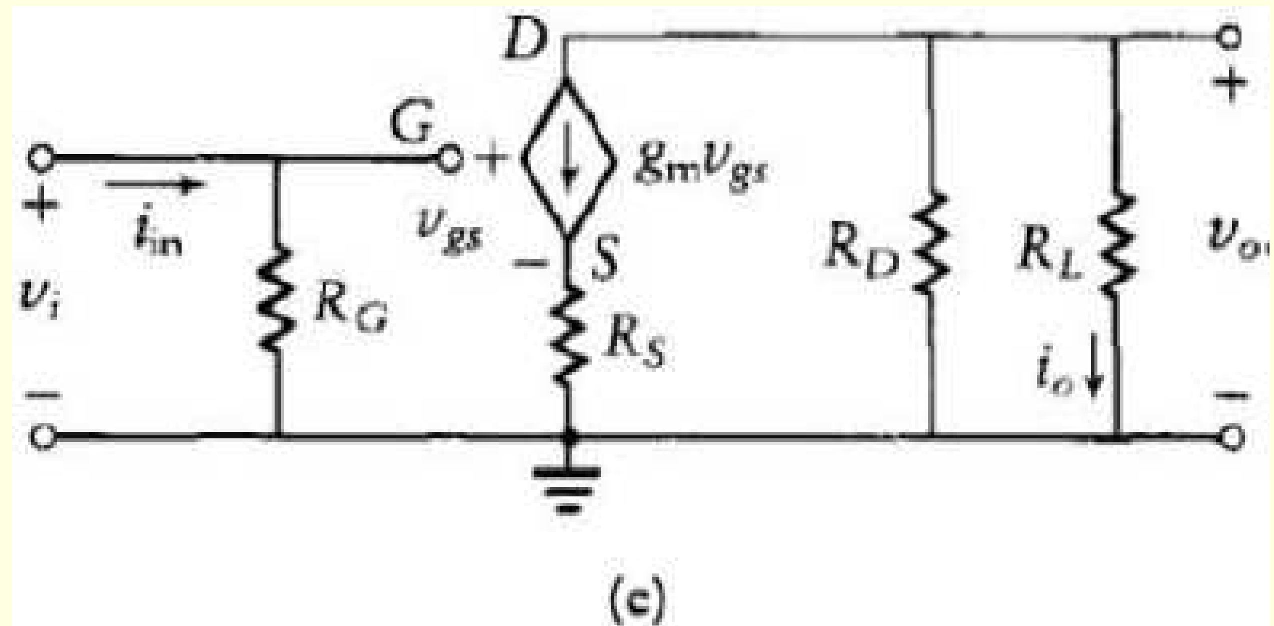
(c)

FET amplifier.

4.6 Analysis of a CS Amplifier

The resistance, R_S, is sometimes bypassed by a capacitor, in which case the voltage gain increases to

$$A_v = -g_m(R_D \parallel R_L)$$



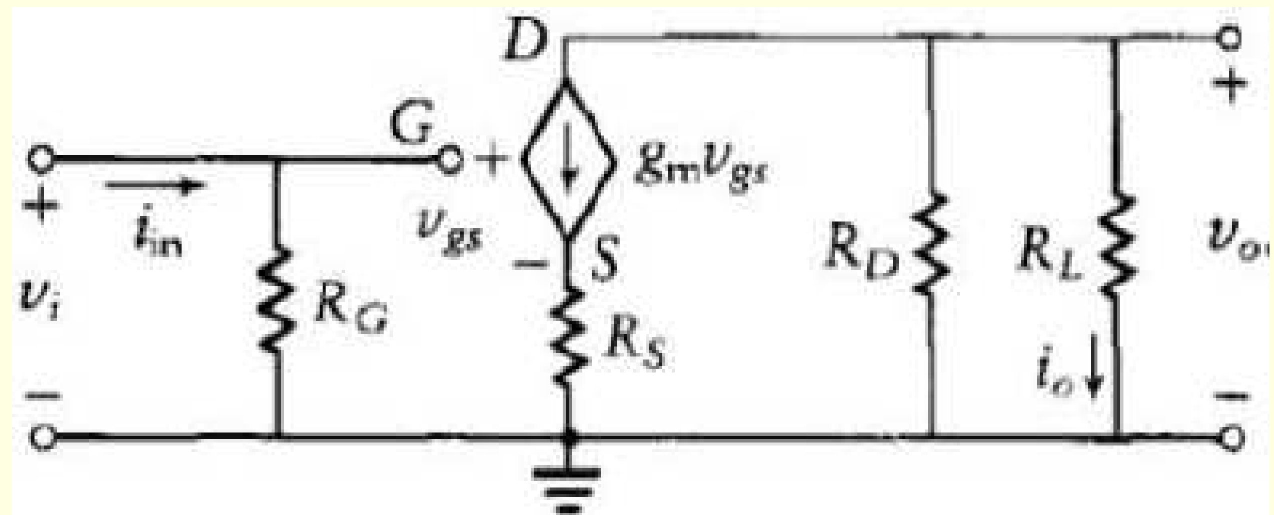
FET amplifier.

4.6 Analysis of a CS Amplifier

The input resistance and current gain are given by

$$R_{in} = R_G = R_1 \parallel R_2 \tag{4.16b}$$

$$A_i = \frac{i_o}{i_{in}} = \frac{A_v R_{in}}{R_L} = \frac{-R_D \parallel R_L}{R_S + 1/g_m} \frac{R_{in}}{R_L} = \frac{-R_G}{R_S + 1/g_m} \frac{R_D}{R_D + R_L} \tag{4.16c}$$

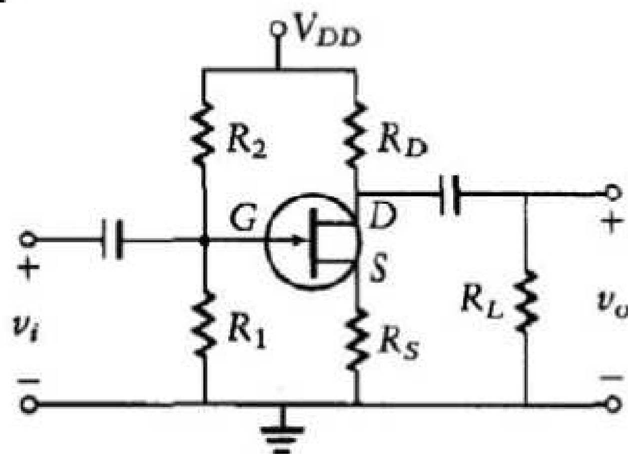


FET amplifier.

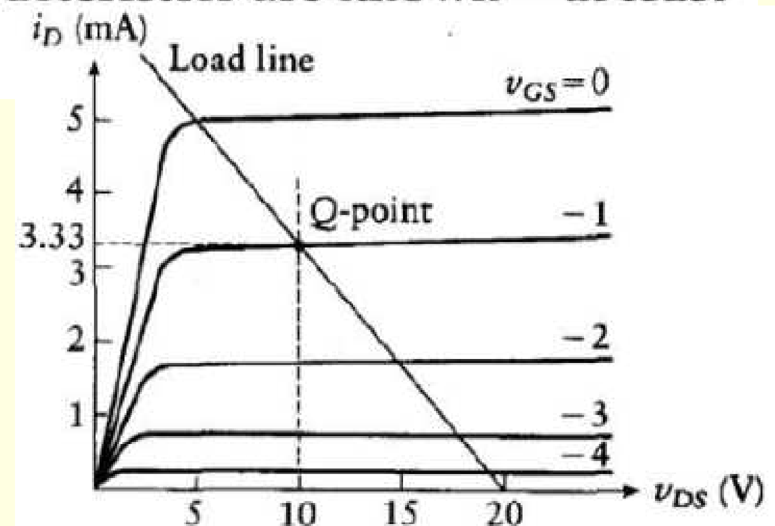
4.7 Design of a CS Amplifier

The design procedure of a CS amplifier is presented in this section. The JFET and the depletion MOSFET amplifier design is presented as a step-by-step procedure. You should convince yourself that you understand the origin of each step, since several variations may subsequently be required.

Amplifiers are designed to meet gain requirements if the desired specifications are within the range of the transistor. The supply voltage, load resistance, voltage gain and input resistance (or current gain) are usually specified. Our problem is to select the resistance values R_1, R_2, R_D, and R_S. Refer to Figure 4.15 as you follow the steps in the procedure. This procedure assumes that a device has been selected and that its characteristics are known—at least V_p and I_{DSS}.



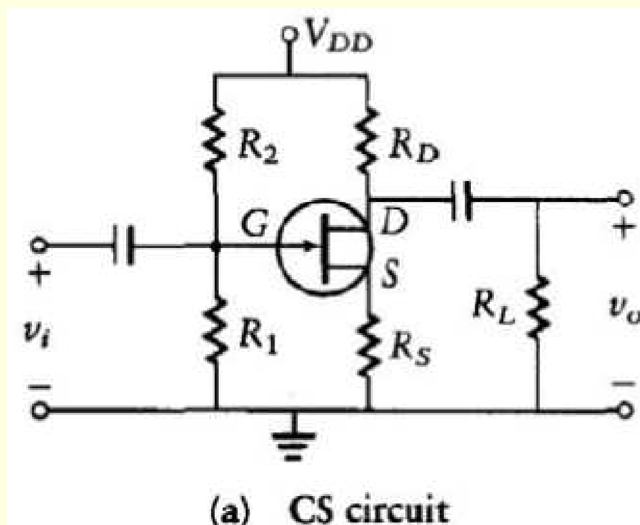
(a) CS circuit



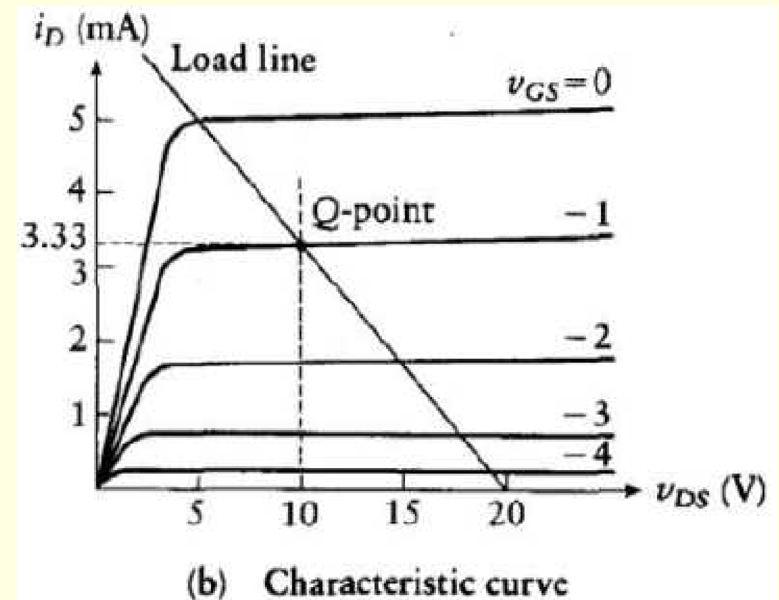
(b) Characteristic curve

4.7 Design of a CS Amplifier

[redacted] If the voltage gain is too high, it may not be possible to effect the design with any Q-point. A different transistor may be needed or the use of two separate stages may be required.



(a) CS circuit



(b) Characteristic curve