Section 1

Introduction and Overview

Purpose:

A programming and system development course for the ADSP-BF533 family that takes a hands-on approach to teaching the architecture, instruction set and development tools.

ADSP-BF533 family refers to the ADSP-BF533 and the ADSP-BF532 and the ADSP-BF531 memory variants. Information specific to the ADSP-BF532/1 parts (e.g. memory variants and performance) is provided when required.

ADSP-BF533 Course Overview

- Introduction and Course Overview
- Introduction to Software Tools
- The Core Computational Units
- The Core DAGs
- The ADSP-BF533 Memory
- The Core Sequencer
- Software Development
- Advanced Instructions/Optimization
- Peripherals – SPORT, SPI, Programmable Flags, UART, Timers, PPI, EBIU
- System Design
- C Compiler
- Hardware Tools
- Questions/Answers

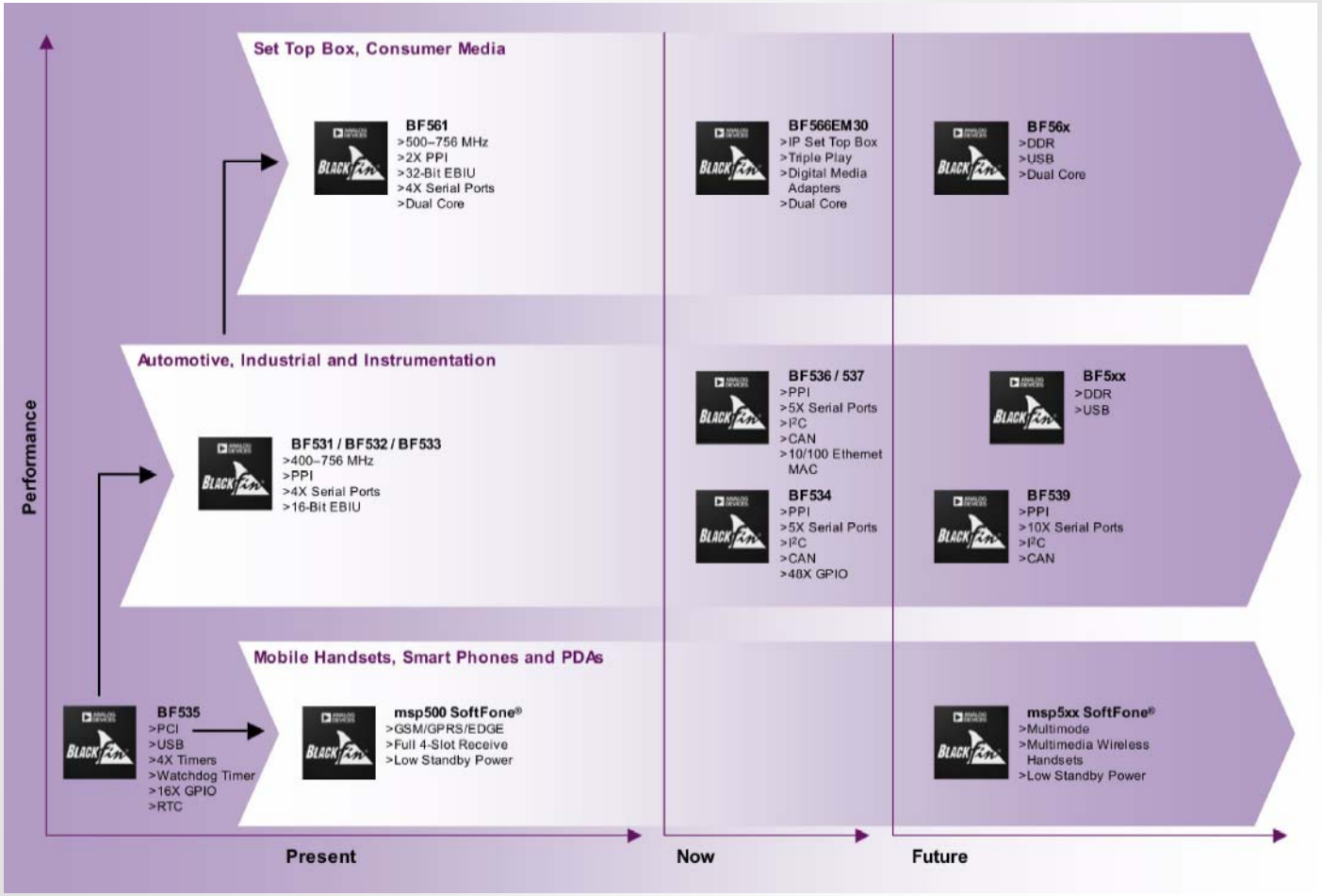
Course Logistics

- Start Time
- Breaks
- Rest Rooms
- Lunch
- Stop Time

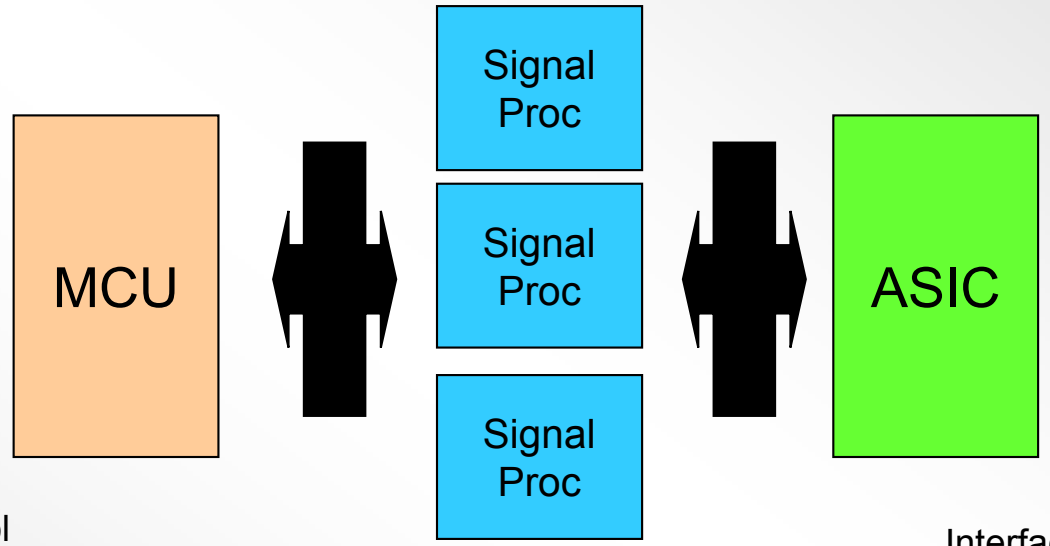
Course Handouts

1. Course Workbook
2. CD with
   a) ADSP-BF533 Hardware Reference
   b) Blackfin™ DSP Instruction Set Reference
   c) Blackfin™ Application Notes
   d) VisualDSP++ Manual Set
      i) Assembler Manual for Blackfin DSP Family
      ii) C Compiler and Library Manual for Blackfin DSP Family
      iii) Debugger Guide and Reference
      iv) Linker and Utilities Manual for Blackfin DSP Family
   e) VisualDSP++ Test Drive
   f) PDF of workshop presentation

Blackfin Processor Roadmap



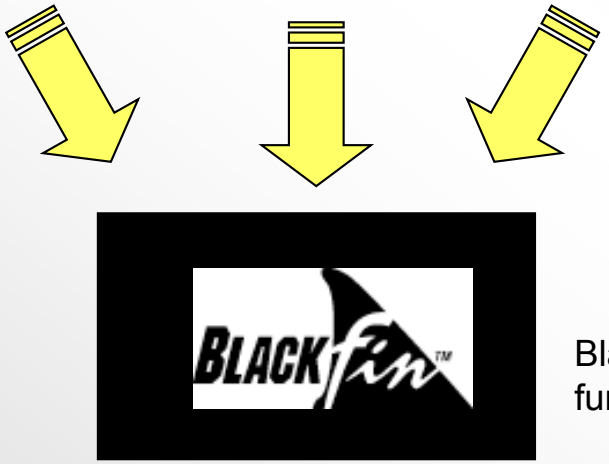
Blackfin Processors Perform Signal Processing and Micro-controller Functions



Traditional model

Control
Networking
RTC
Watchdog
RTOS
MMU
Byte addressable

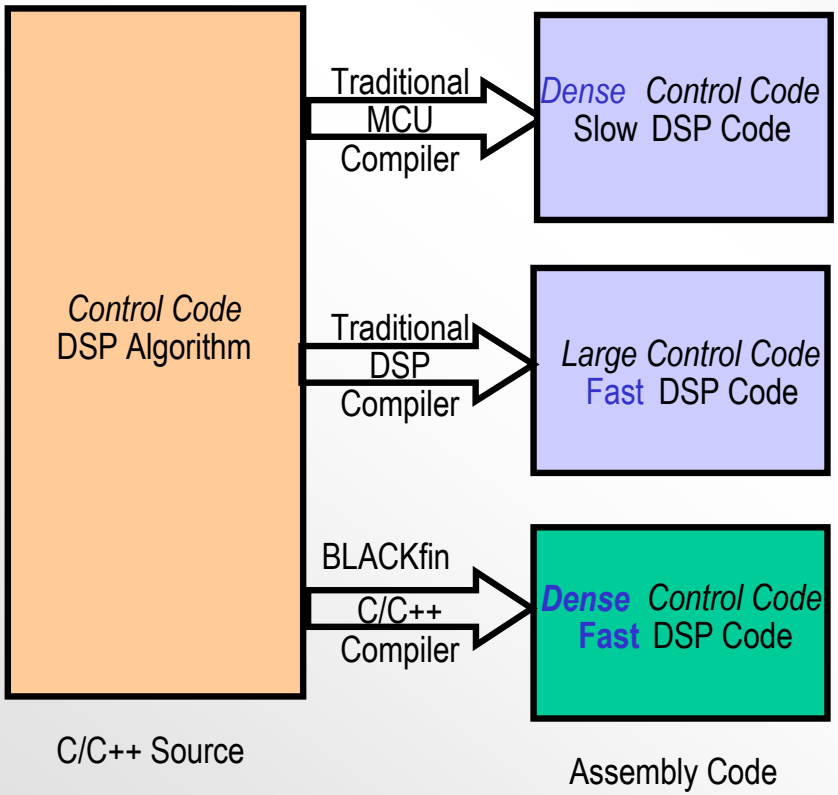
Interfaces to sensors
Broad peripheral mix
Memory



New model

Blackfin can perform all of these functions

What are the characteristics of a Good Embedded Processor?



Traditional MCU Compiler generates

- Dense control code, BUT
- Much larger and slower DSP code

Traditional DSP Compiler generates

- Good DSP algorithm code, BUT
- Much larger control code

Architecture and Compiler Work Together to Deliver Dense Control Code and Fast DSP Code

ADSP-BF533 Controller Features

- Dedicated L1 memory space for Stack & Heap
- Dedicated Stack and Frame Pointers
- Dedicated bank of general purpose pointer registers
- Enhanced Data Address Generators
- Byte addressability
- Instruction set that is compiler friendly
- Very large linear address map
- Simple bit level manipulation

What are the characteristics of a Good DSP?

- Fast, flexible arithmetic computation units
- Unconstrained data flow to and from the computation units
- Extended precision and dynamic range in the computation units
- Efficient program sequencing
- Ease of programming
- Efficient I/O Processing

ADSP-BF533 Core DSP Features

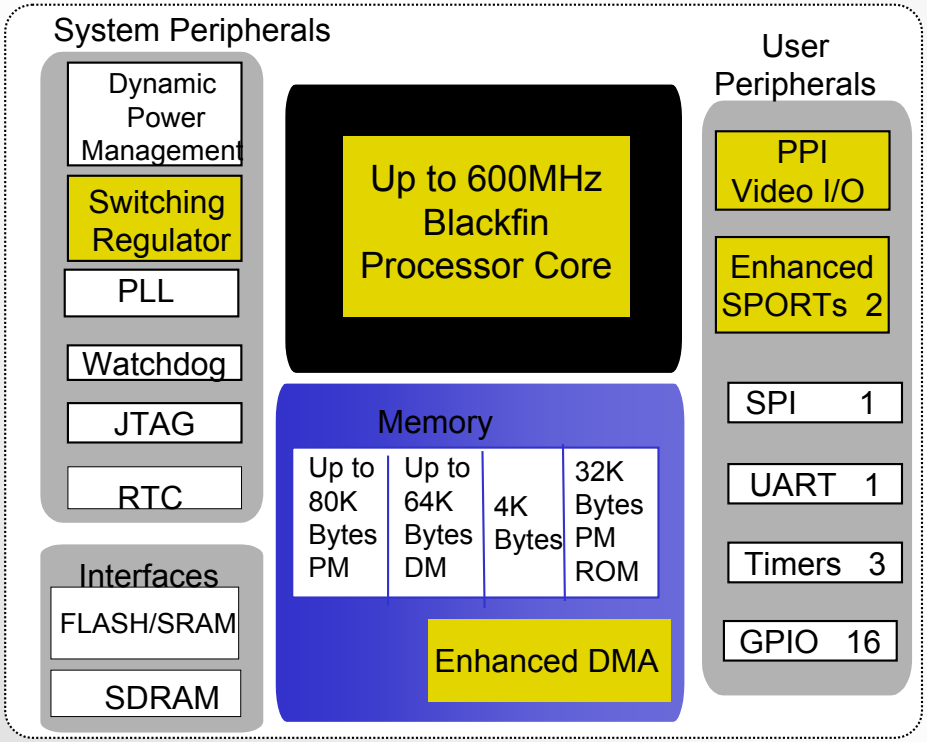
- Fixed point DSP math
  - Dual 32/40-bit Data ALUs with 40-bit Accumulators
  - Dual 16-bit MACs
  - Dual 32-bit Data Address Generator (DAG)
    - Conventional addressing modes for C code
- Modified-Harvard memory architecture
  - Two data ports and one code port to a unified memory space
- Configurable hierarchical data and instruction memories
  - Cache and/or SRAM
- Instruction set optimizations
  - Easy to use algebraic syntax
  - Video-specific instructions

ADSP-BF533/BF532/BF531

- The BLACK*fin* family offers a variety of pin- and code-compatible derivatives

	ADSP - BF531	ADSP - BF532	ADSP - BF533
Performance	300, 400 MHz, 600, 800 MMACs	300, 400 MHz, 600, 800 MMACs	500, 600 MHz, 1000, 1200 MMACs
On Chip RAM	52 KBytes	84 KBytes	148 KBytes
Package Options	LQFP, MiniBGA	LQFP, MiniBGA	MiniBGA

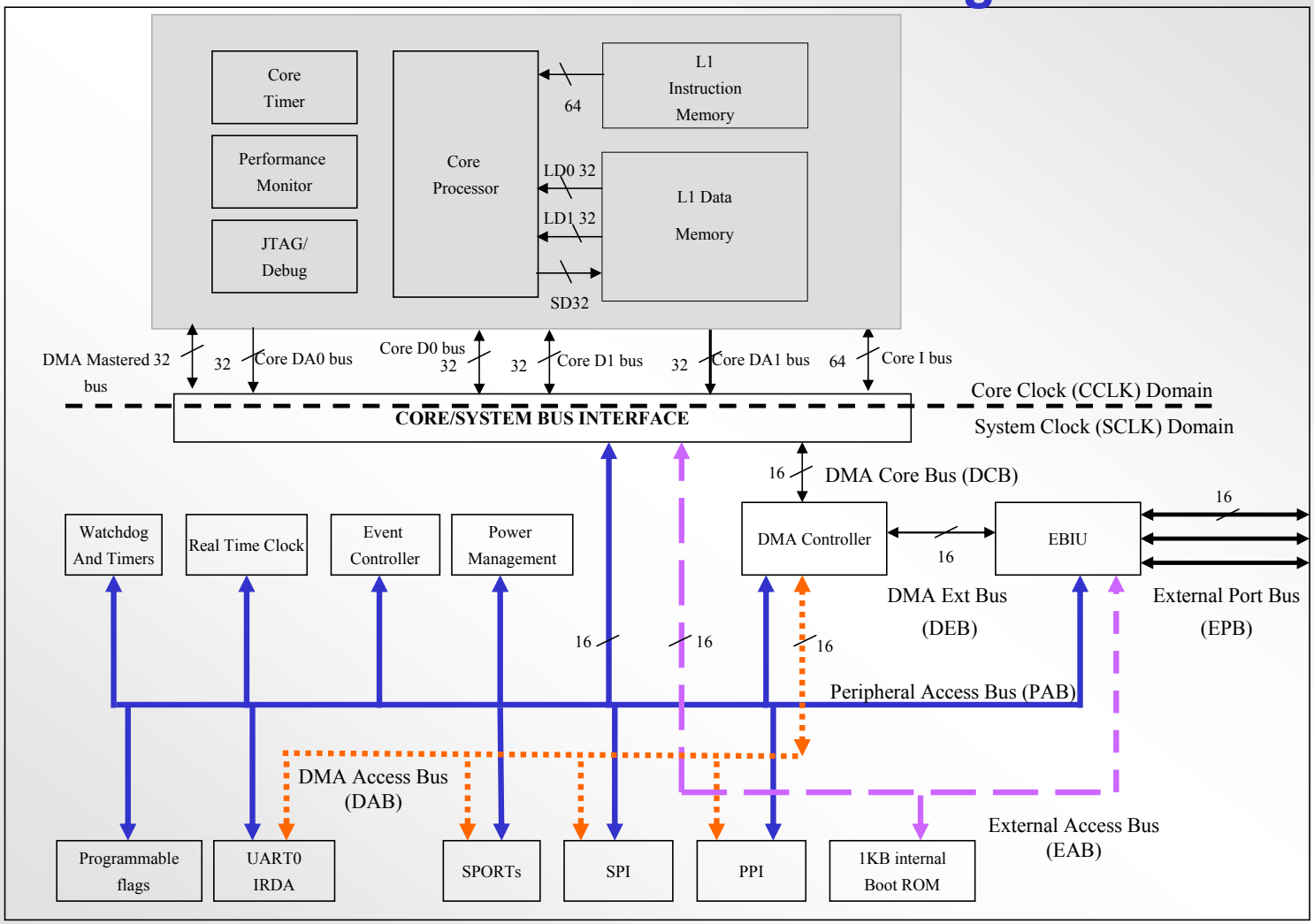
ADSP-BF533/BF532/BF531
Enhanced Blackfin Processors



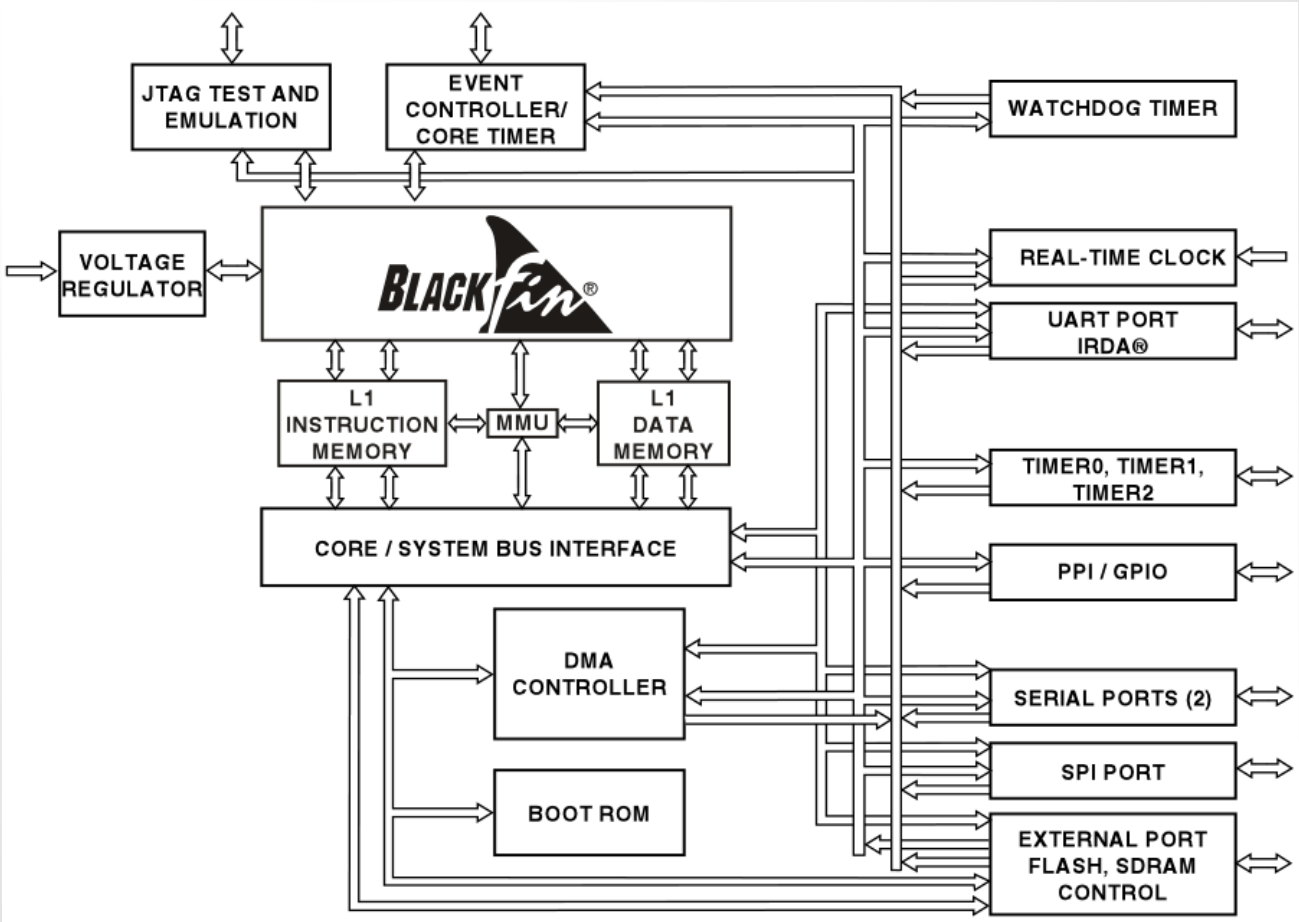
- **High System Integration**
  - Video I/O connects directly to ITU-R 656 encoders and decoders
  - SPORTs support 8 Channels of I^2S Audio
  - Core Voltage Regulator
  - Microcontroller features include WDT, RTC, SDRAM controller

New Blackfin features

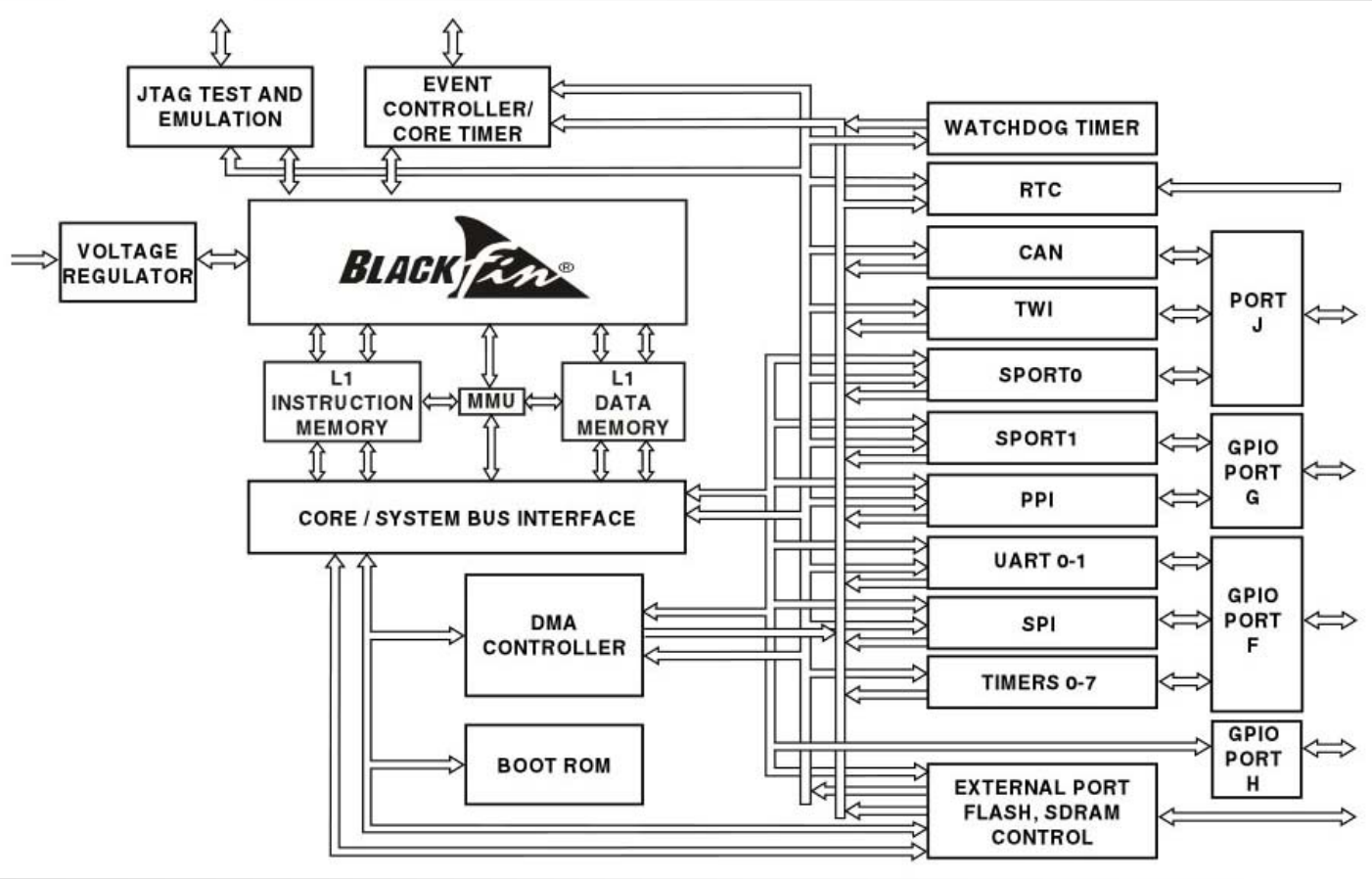
ADSP-BF533 Block Diagram



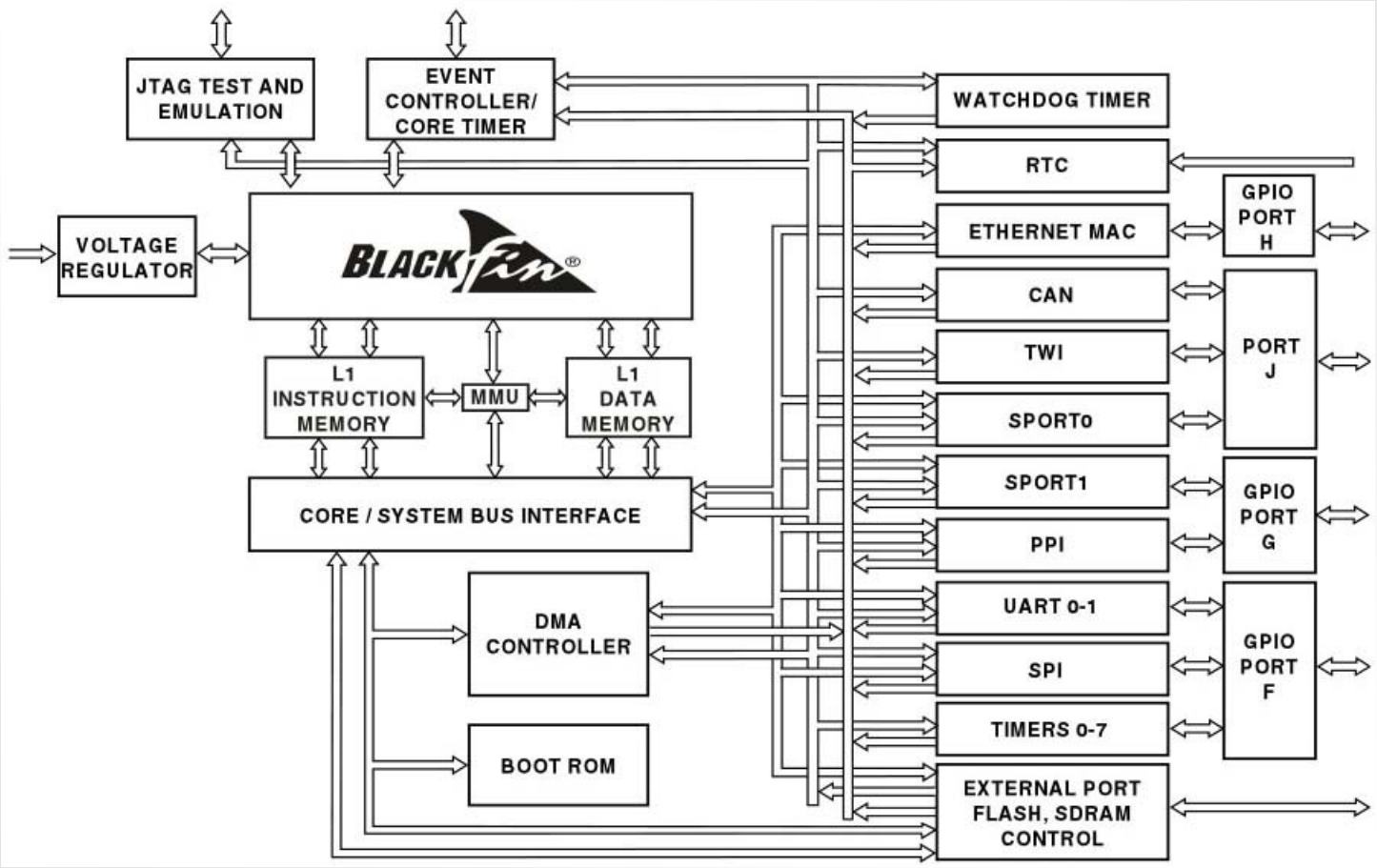
ADSP-BF533/2/1



ADSP-BF534


JTAG TEST AND EMULATION
EVENT CONTROLLER/ CORE TIMER
VOLTAGE REGULATOR
BLACKfin
L1 INSTRUCTION MEMORY
MMU
L1 DATA MEMORY
CORE / SYSTEM BUS INTERFACE
DMA CONTROLLER
BOOT ROM
WATCHDOG TIMER
RTC
CAN
TWI
SPORT0
SPORT1
PPI
UART 0-1
SPI
TIMERS 0-7
EXTERNAL PORT FLASH, SDRAM CONTROL
PORT J
GPIO PORT G
GPIO PORT F
GPIO PORT H

ADSP-BF536/7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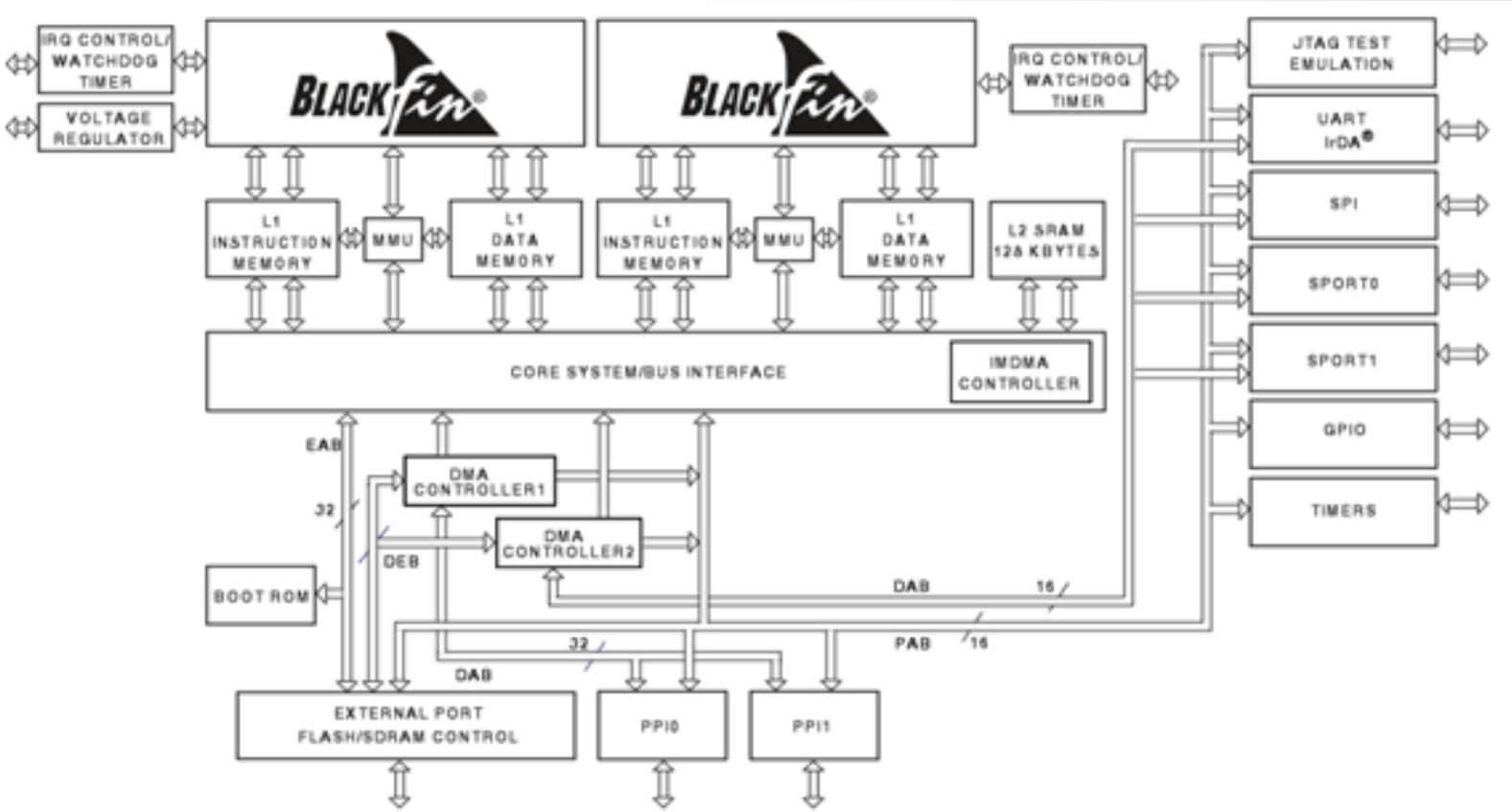
WATCHDOG TIMER
RTC
ETHERNET MAC
CAN
TWI
SPORT0
SPORT1
PPI
UART 0-1
SPI
TIMERS 0-7
EXTERNAL PORT FLASH, SDRAM CONTROL
GPIO PORT H
PORT J
GPIO PORT G
GPIO PORT F

ADSP-BF561


IRQ CONTROL/ WATCHDOG TIMER
VOLTAGE REGULATOR
BLACKfin
BLACKfin
IRQ CONTROL/ WATCHDOG TIMER
JTAG TEST EMULATION
UART IrDA®
SPI
SPORT0
SPORT1
GPIO
TIMERS
L1 INSTRUCTION MEMORY
MMU
L1 DATA MEMORY
L1 INSTRUCTION MEMORY
MMU
L1 DATA MEMORY
L2 SRAM 128 KBYTES
CORE SYSTEM/BUS INTERFACE
IMDMA CONTROLLER
EAB
32
DEB
DMA CONTROLLER1
DMA CONTROLLER2
BOOT ROM
DAB
16
PAB
16
32
DAB
EXTERNAL PORT FLASH/SDRAM CONTROL
PPI0
PPI1

ADSP-BF533 Clock Definitions

- There are two internal clock domains:
  - Core Clock (CCLK) is the rate of instruction execution and the rate of the internal memory speed
  - System Clock (SCLK) is the clock which is used to derive some peripheral clocks. The DMA Controller and the external memory bus both run at SCLK

Operating Mode Summary

- The Blackfin Processor has 3 different operating modes to support both traditional DSP applications and embedded-RTOS applications:
  - Supervisor mode
    - Allows full access to all peripheral resource
    - May be used for O/S kernel, device drivers
    - Must be servicing an interrupt or exception to be in Supervisor mode
  - User mode
    - Algorithm code that shouldn't access peripheral resources
    - Must not be servicing an interrupt or exception to be in User mode
  - Emulator (or Debug) mode
    - Has supervisor abilities and is accessible via JTAG

Some applications may simply run in Supervisor mode all the time.