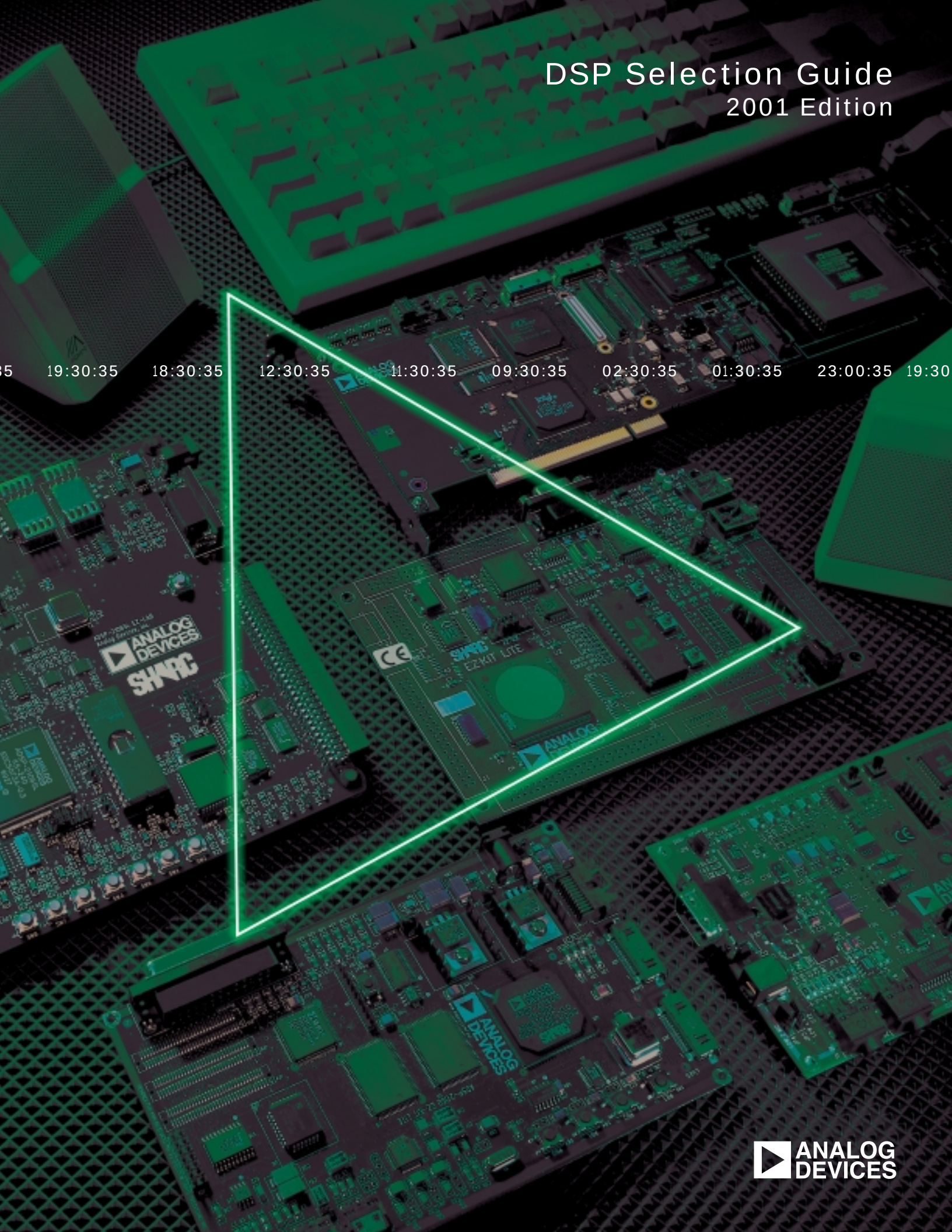
DSP Selection Guide

2001 Edition



ANALOG DEVICES

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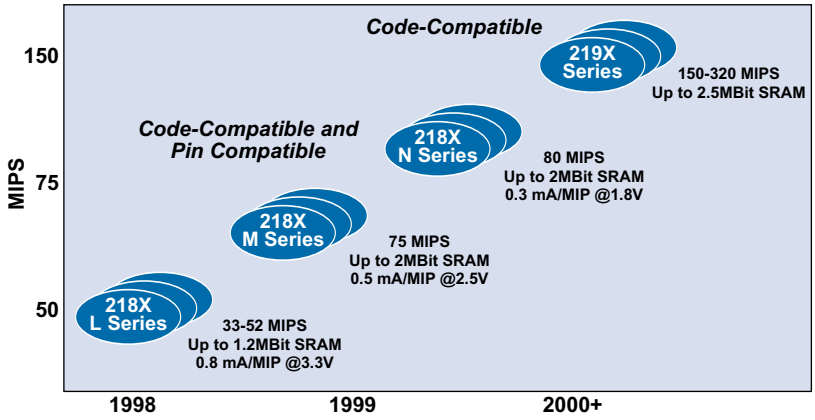
16-Bit DSP Key Products
Recommended for New Designs



16-Bit Generic	Package	Max MIPS	Vcc	Program RAM Words	Data RAM Words	Status	Price*
ADSP-2192	ST	320	2.5V	32K	100K	Samples Mar-01 Release 3Q01	$53.20
ADSP-2188M	ST, CA	75	2.5V	48K	56K	Released	$28.00
ADSP-2188N	ST, CA	80	1.8V	48K	56K	Samples Now Release 2Q01	$26.00**
ADSP-2189M	ST, CA	75	2.5V	32K	48K	Released	$23.00
ADSP-2189N	ST, CA	80	1.8V	32K	48K	Samples Now Release 2Q01	$21.00**
ADSP-2187N	ST, CA	80	1.8V	32K	32K	Samples Now Release 2Q01	$17.00**
ADSP-2185M	ST, CA	75	2.5V	16K	16K	Released	$10.00
ADSP-2185N	ST, CA	80	1.8V	16K	16K	Samples Now Release 2Q01	$9.50**
ADSP-2186M	ST, CA	75	2.5V	8K	8K	Released	$7.50
ADSP-2186N	ST, CA	80	1.8V	8K	8K	Samples Now Release 2Q01	$7.25**
ADSP-2184N	ST, CA	80	1.8V	4K	4K	Samples Now Release 2Q01	$5.75**

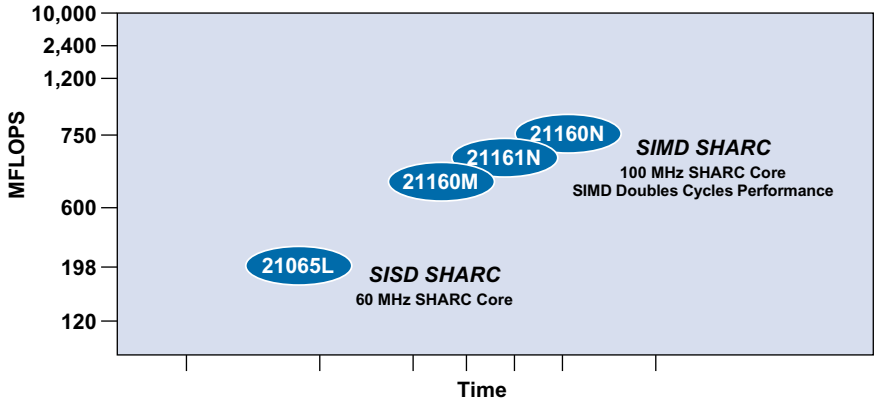
Packages: ST = Thin Quad Flat Pack (TQFP)
CA = Mini Ball Grid Array (10 x 10 mm)

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities

** Budgetary pricing – subject to change

Processor	Evaluation Development Platform	Emulator	Development Software
ADSP-218xM	ADDS-2189M-EZLITE $295	ADDS-218X-ICE-1.8V $1995	VDSP-21XX-PC-FULL $2995
ADSP-218xN	ADDS-2189M-EZLITE $295	ADDS-218X-ICE-1.8V $1995	VDSP-21XX-PC-FULL $2995
ADSP-2192	ADDS-2192-12EZLITE $295	ADDS-APEX-ICE $4995 ADDS-TREK-ICE $5995 ADDS-SUMMIT-ICE $3995	VDSP-21XX-PC-FULL $2995

32-Bit SHARC® DSP Key Products
Recommended for New Designs



32-Bit Generic	Package	Max MFLOPS	Vcc	On-Chip SRAM	Status	Price*
ADSP-21160N	B	540	1.9/3.3V	4 Mbits	Samples 4Q01	$145.00
ADSP-21160M	B	480	2.5/3.3V	4 Mbits	Released	$145.00
ADSP-21065L	S, B	198	3.3V	544 Kbits	Released	$30.00
ADSP-21161N	B	600	1.8/3.3V	1 Mbits	Samples 2Q01 Released 1Q02	$34.32

Packages: B = Plastic Ball Grid Array (PBGA)
S = Plastic Quad Flat Pack (PQFP)

* US Dollars. Lowest grade suggested resale price per unit in 1000 unit quantities

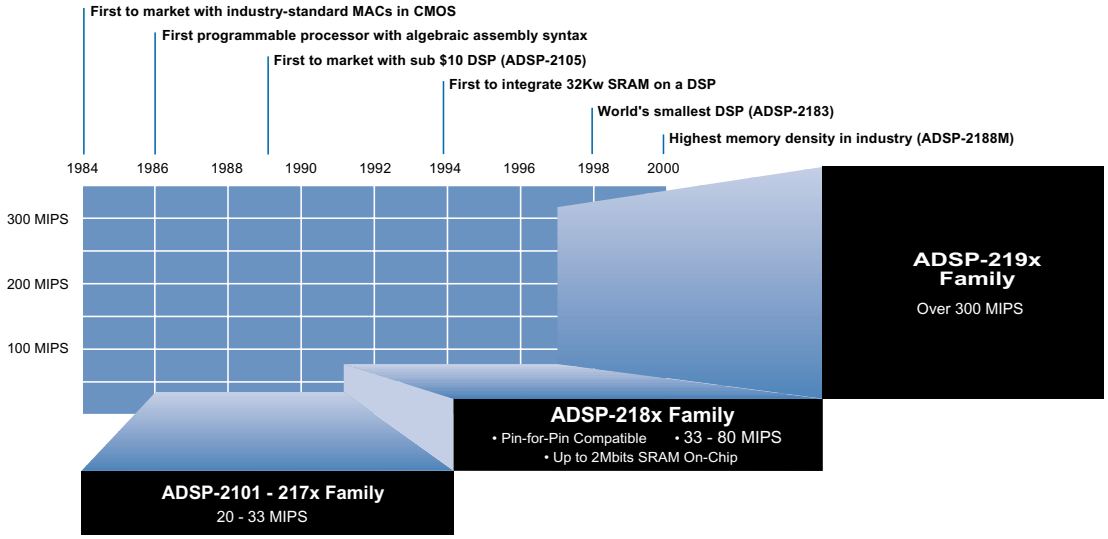
Processor	Evaluation Development Platform	Emulator	Development Software
ADSP-21065L	ADDS-21065L-EZLITE $299	ADDS-APEX-ICE $4995 ADDS-TREK-ICE $5995 ADDS-SUMMIT-ICE $3995	VDSP-SHARC-PC-FULL $2995
ADSP-21160M	ADDS-21160M-EZLITE $595	ADDS-APEX-ICE $4995 ADDS-TREK-ICE $5995 ADDS-SUMMIT-ICE $3995	VDSP-SHARC-PC-FULL $2995
ADSP-21161N	ADDS-21161N-EZLITE TBD (Available 2Q01)	ADDS-APEX-ICE $4995 ADDS-TREK-ICE $5995 ADDS-SUMMIT-ICE $3995	VDSP-SHARC-PC-FULL $2995

ADI DSP Overview
Architectural Roadmaps

Analog Devices is the world's fastest-growing DSP supplier. Our portfolio includes mixed-signal DSPs, general-purpose DSPs, such as the SHARC® family, and embedded DSP solutions that serve secure data, ADSL modems, GSM handsets, internet access, speech processing and motor control applications. ADI leverages 30 years of high performance analog expertise to develop DSPs that make the design challenge easier. ADI's DSP architectures feature simple, yet powerful programming models and are supported by the White Mountain brand of high-quality development tools. More than 30,000 software developers have invested in our 16-bit and 32-bit fixed-point and floating-point DSP architectures.

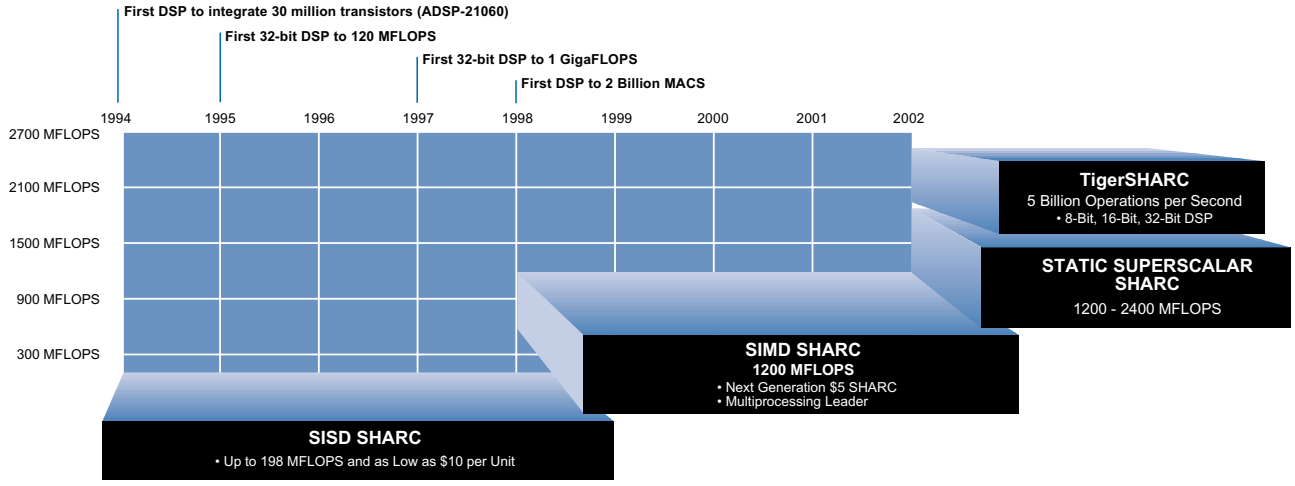
Analog Devices ADSP-2100 16-Bit DSP Roadmap

The ADSP-2100 family has inspired thousands of high-performance applications at the forefront of DSP integration. All DSPs in the ADSP-2100 family share the same base architecture and algebraic assembly language. The trademark simplicity of the assembly programming language makes learning code, reading code, and using code very easy. More memory, faster processing, and lower power consumption have made these workhorses the right choices in more than 10,000 designs. Our commitment to meeting our customers' production needs will keep applications of 16-bit DSPs growing strong.



Analog Devices ADSP-21000 SHARC 32-Bit DSP Roadmap

The SHARC family of fixed- and floating-point 32-bit processors has successfully defined a new standard in overall DSP integration. By placing an emphasis on balance – between computational core performance, memory bandwidth, and I/O throughput – SHARC DSP performance is predictably high and sustained.



DSP Markets and Applications

As the processing capabilities of DSPs have increased, they are being used in more and more applications.

The integration of DSPs into a wide range of applications is simplified by the availability of runtime libraries (included with the C compiler). ADI's Applications Engineering group and our third party solutions providers have prepared code for many key algorithms.

Audio Signal Processing

DSP Function	Application
• Reverb • Tone Control • Echo • Filtering • Audio Compression • Frequency Equalization • Pitch Shifting • Spatial Effects • Surround Sound	• Musical Instruments & Amplifiers • Audio Mixing Consoles • Recording Equipment • Disc Jockey Mixing Consoles • Broadcast Equipment • Cable TV Equipment • Audio Equipment & Boards for PCs • Toys & Games • Automotive Sound Systems • Digital Audio Tape Players • Compact Disk Players • HDTV Equipment • Digital TV

Recommended DSPs

- ADSP-21065L
- ADSP-21160M
- ADSP-21161N

Speech Processing

DSP Function	Application
• Speech Synthesis • Speech Recognition • Speech Compression • Text to Speech • Pitch Shifting • Filtering • Speech Record & Playback	• Digital Tapeless Recorders • Voice Store Equipment • Phone Mail • Voice Secure Entry Systems • Intercom Systems • Personal ID Systems • Audio Equipment & Boards for PCs • Toys & Games

Recommended DSPs

- ADSP-218XM/N
- ADSP-21065L
- ADSP-21161N

Communications

DSP Function	Application
• Modulation & Transmission • Demodulation & Reception • Speech Compression • T1 Switching • DTMF • Data Encryption • Signal Recovery • Echo Cancellation • Voice Over Data	• Modems • Fax Machines • PBX Systems • Phone Mail Systems •Private Data Communications Systems • Automatic Teller Machines • Broadcast Equipment • Mobile Phones • Digital Pagers • Global Positioning Systems • Secure, Speaker, & Video Telephones • Digital Answering Machines • Satellite Phones • Wireless Local Loop • Telecom Infrastructure

Recommended DSPs

- ADSP-218XM/N
- ADSP-21065L

Instrumentation and Measurement

DSP Function	Application
• Fast Fourier Transform (FFT) • Filtering • Waveform Synthesis • Adaptive Filtering • High Speed Numeric Calculations	• Test & Measurement Equipment • Vibration Analysis Equipment • I/O Cards for PCs • Automotive Engine Analyzers • Automotive Wheel Balancers • Industrial Scales & Measurement • Active Mufflers • Oil Drilling Equipment • Seismic Instruments • Power Meters • Exercise Machines • Signal Analyzers • Function/Signal Generators

Recommended DSPs

- ADSP-218XM/N
- ADSP-21065L
- ADSP-21161N

Medical Electronics

DSP Function	Application
• Filtering • Echo Cancellation • Fast Fourier Transform (FFT) • Beam Forming	• Respiration Monitoring Equipment • Heart Rate/Cardiac Monitoring • Ultra Sound Equipment • Medical Imaging Equipment • Blood Analyzers • Fetal/Infant Monitors • Patient Monitors • Blood Flow Monitors • CAT Scanners • Hearing Aides

Recommended DSPs

- ADSP-218XM/N
- ADSP-2116X
- ADSP-2106X

Optical and Image Processing

DSP Function	Application
• 2-Dimensional Filtering • Fast Fourier Transform (FFT) • Pattern Recognition • Image Smoothing	• Bar Code Scanners • Underwater Object Finders • Automatic Inspection Systems • Fingerprint Recognition • Digital Televisions • Sonar/Radar Systems • Robotic Vision • Vision Systems

Recommended DSPs

- ADSP-2106X
- ADSP-2116X

Industrial/Motor Control

DSP Function	Application
• Filtering • Fast Fourier Transform (FFT) • Control Loops • Noise Cancellation	• Motors in Appliances, Robotics or Office Automation • Power Management Equipment • Generators • Elevators • Air Conditioners • Traffic Control Systems • Navigation • Disk Drives • High Speed Controls • Vibration Analyzers

Recommended DSPs

- ADSP-2106X
- ADSP-21160M
- ADMCXXX
- ADSP-218XM/N

ADI DSP Key Benefits

Selecting a DSP processor can be a difficult task. Design engineers are concerned with time-to-market, for which ease of use, quality development tools, extensive application engineering support, and the availability of algorithm code are critical. Of course, designers are also concerned with low production cost, low power consumption, system integration, and other criteria such as clock frequency, size of on-chip memory, and high-level language support. To understand the benefits of ADI's families of 16- and 32-bit DSPs and how ADI's architectures are optimized for digital signal processing, keep in mind three basic features of DSP. DSPs must have the ability to:

1) Perform fast arithmetic
2) Fetch data at a fast rate
3) Sequence efficiently through repetitive operations

Key Feature	Benefit
Single Cycle Instruction Execution	• One cycle per instruction execution • ADSP-218x requires no extra latency cycles for decision branches, condition code checking, or subroutine calls • Delayed branches increase efficiency on pipelined architectures such as SHARC and ADSP-219x • Deterministic operations make it easy to develop, profile, and benchmark code
Code Compatible Family Members	• All ADSP-2100 Family members share the same base architecture and assembly language • All ADSP-21000 SHARC Family members share the same base architecture and assembly language • No need to learn or invest in new development tools when moving from one family member to another • Software investment is preserved
Simple Programming Language	• Algebraic syntax assembly language makes code easy to use, easy to learn, and easy to read • Unlike competitors who use mnemonics like SPAC and XORX, ADI assembly language syntax makes programming in highly-efficient assembly language easy
Balanced Core, Memory and I/O Integration	• Fast core processing, large on-chip memories, and high bandwidth I/O simplify real-time system development • Up to 14 channels of non-intrusive Direct Memory Access (DMA) allow data movement without interrupting math processing
Large On-Chip Memory	• Provides ample on-chip storage for most common DSP tasks such as digital filtering and FFTs, eliminating the need for off-chip memory
Efficient Program Sequencing and Zero-Overhead Looping	• Minimizes off-chip memory access wait states • On-chip hardware manages looping and provides the most efficient code execution with no extra programming for repetitive DSP code • No need to control looping with complex software
Pin-for-Pin Compatible Family Members	• Increase speed or memory integration within a common pin-out • Adds flexibility without requiring board redesign

ADI DSP Common Features

All Family Members Share These Common Features

- Single-cycle instruction execution
- Separate program and data buses on-chip
- Dual-purpose program memory for both instruction and data storage
- Three independent computation units: ALU, multiplier/accumulator, and barrel shifter
- Two independent data address generators
- Powerful program sequencer provides:
  - Zero overhead looping
  - Conditional arithmetic instruction execution
- Programmable wait state generation
- Automatic booting of internal program memory from low cost byte-wide external memory or other sources. (e.g., EPROM or host interface port)
- Single-cycle context switch
- Multifunction instructions
- Edge- or level-sensitive external interrupts
- Rich instruction set, conditional execution
- Nestable, interruptible hardware circular buffers
- Shadowing of most arithmetic registers with single-level, single-cycle register set context switch
- Support for operand-unrelated parallel moves, including register-to-register moves
- Barrel shifter supports shifting by 0-32 bits
- Large number of address registers
- Support for modulo and bit-reversed addressing

VisualDSP++™
Integrated Development Environment

Features

Integrated Development Environment

- Define all project and tool configurations through property page dialog boxes
- Set project-wide or individual file settings for debug or release mode project builds
- Create source files using an integrated, full-featured editor with syntax highlighting, OLE drag and drop, and bookmarks

Debugger

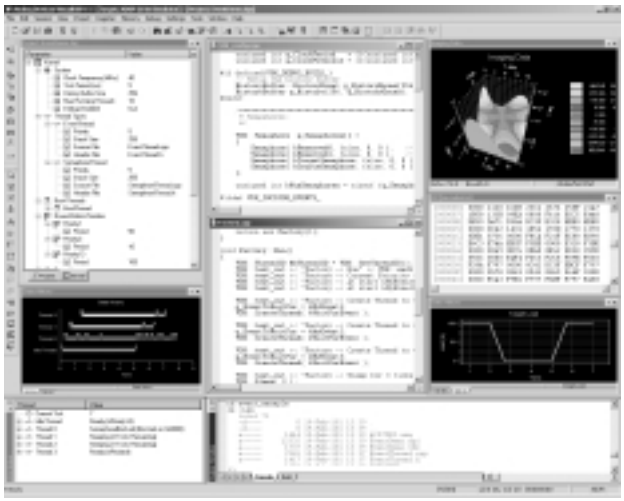
- View source files in C/C++, assembly, or mixed C and assembly
- Profile and trace instruction execution of C/C++ and assembly programs (simulation only)
- Set watch points (conditional breakpoints) on processor registers and stacks, as well as program and data memory including:
  - Inclusive or exclusive memory range
  - Read or write of any value or a specific value
  - Stack overflows and underflows
- Create custom register windows
- Simulate standard I/O, interrupts, and streams (simulator only)
- Statistical profiling
- MP (multiprocessing)
- Graphical plotting

Code Generation Key Features

- Program with an easy-to-use, algebraic syntax assembly language
- Develop applications using an optimizing C/C++ compiler
- Intersperse inline assembly statements within C/C++ source code
- Create executables using a linker that supports multiprocessing, shared memory, and code overlays
- Access numerous math, DSP, and C/C++ runtime library routines
- Create host, link port, and PROM boot images
- Initialize all data and code memory locations using modifiable loader
- Concantenate multiple executables within single PROM image

Overview

VisualDSP++™ is an easy-to-use project management environment, comprised of an integrated development environment (IDE) and debugger. VisualDSP++ enables management of projects from start to finish from within a single interface. The project development and debug environments are integrated, allowing movement easily between editing, building, and debugging activities.



VisualDSP++ debugger interface

Platform and Processor Support

VisualDSP++ supports the SHARC® DSP family on Windows® 9x, Windows NT, and Windows 2000. ADSP-218x (ADSP-218x does not have C++) and ADSP-219x families will be available soon.

Flexible Project Management

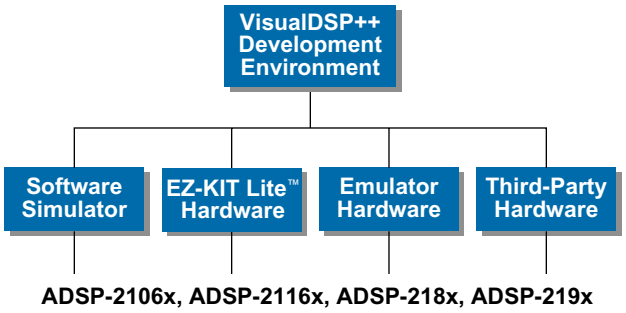
The IDE provides flexible project management for the development of DSP applications. The IDE includes access to all the activities necessary to create and debug DSP projects. The IDE editor allows the creation or modification of source files or viewing of listing or map files. This powerful editor is part

of the IDE and includes multiple language syntax highlighting, OLE drag and drop, bookmarks, and standard editing operations such as undo/redo, find/replace, copy/paste/cut, and go to.

The IDE allows access to the DSP C/C++ compiler, C/C++ runtime library, assembler, linker, loader, and splitter. Specification of options for these tools is made possible through the property page dialogs. Property page dialogs are easy to use and simplify configuring, changing, and managing projects. These options may be defined once and then modified to meet changing development needs. The DSP code generation tools can be accessed from the operating system command line.

Greatly Reduced Debugging Time

The VisualDSP++ debugger has an easy-to-use, common interface to all DSP simulators and emulators available through Analog Devices, Inc. (ADI) and many from participating parties.



VisualDSP++ simplifies DSP development via common development environment across all ADI hardware and DSPs

The debugger has many features that greatly reduce debugging time. C/C++ source can be viewed interspersed with the resulting assembly code. Users can profile execution of a range of instructions in a program; set watch points on hardware and software registers, program and data memory; and trace instruction execution and memory accesses. These features enable users to correct coding errors, identify bottlenecks, and examine DSP performance. The custom register option allows developers to select any combination of registers to view in a single window. The debugger, when used with the simulator, can also generate inputs, outputs, and interrupts to simulate real world application conditions. With C++ developers can realize a significant increase in time to market with the ability to efficiently work with complex signal processing data types and take advantage of specialized DSP operations without having to understand the underlying DSP architecture.

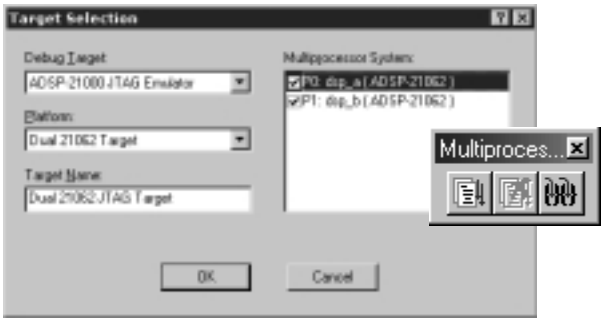
VisualDSP++ simplifies DSP development via common development environment across all Analog Devices hardware and DSPs.

TCL Command Line interface

Tool command line (Tcl) scripting language facilitates executing repeated sequences of debugger commands. This powerful C-like interface allows developing complete test applications of DSP systems.

Multiprocessing Support

VisualDSP++'s smart multiprocessor (MP) debug support provides a seamless interface to multiple DSPs on the same physical hardware. Users are able to issue parallel step, run, and halt commands to all of the applicable DSPs.



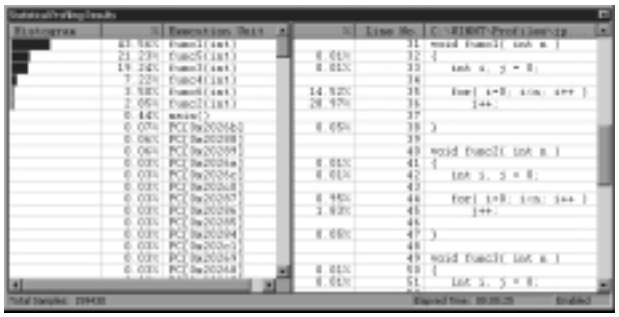
VisualDSP++'s multiprocessor dialog box and tollbar

VisualDSP++

The developer can pick and choose individual DSP register or memory sets of interest by pinning those that should be updated between runs, halts and steps. This feature also eliminates screen clutter in multiprocessor debugging

Statistical Profiling

Statistical profiling allows for a more generalized form of profiling that JTAG emulator debug targets can take advantage of. The debugger has the ability to unintrusively randomly sample the target processors PC and then present the user with a graphical display of the resultant samples. This allows the user to easily see where their application is spending most of its time.



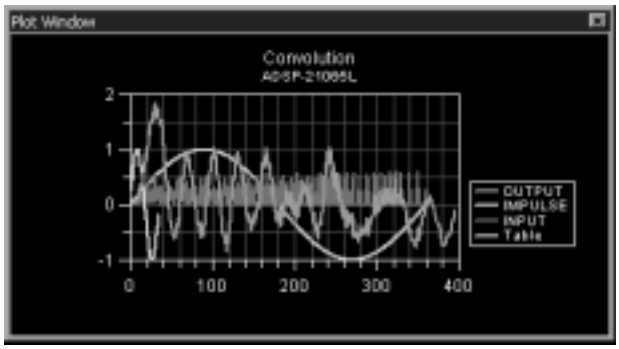
VisualDSP++'s statistical profiling window

Graphical Profiling

The plot window supports exporting images to both bitmap and JPEG format files and has highly configurable formatting options such as title, subtitle, font size, font face, font color and element colors.

Code Generation Tools

DSP code generation tools allow development of applications that take full advantage of the DSPs architecture, including multiprocessing, shared memory, and memory overlays. Code generation tools include the C/C++ compiler, C/C++ runtime library, DSP and math libraries,



VisualDSP++'s plot window

assembler, linker, loader and splitter. Code generation tools work seamlessly within the VisualDSP++ environment.

C/C++ Compiler and Assembler

The C/C++ compiler generates efficient code that is optimized for both code density and execution time. The C/C++ compiler can be easily interfaced with assembly code modules. Thus, users can program in C/C++ and still use assembly for time-critical loops. The math, DSP, and C/C++ runtime library routines help shorten time to market. The SHARC DSP, ADSP-218x (ADSP-218x does not have C++) and ADSP-219x DSP family assembly language is based on an algebraic syntax that is easy to learn, program, and debug. The add instruction, for example, is written in the same manner as the actual equation: the algebraic statement r = x + y is coded in assembly language as

f0 = f1 + f2 (SHARC DSPs example)

Linker & Loader

The linker provides flexible system definition through linker description files (.ldf). In a single .ldf file users are able to define different types of executables for a single or multiprocessor system. The linker resolves symbols over multiple executables, maximizes memory use, and allows common code to be

shared among multiple processors. The loader supports creation of host, link port, and PROM boot images. Along with the linker, the loader allows multiprocessor system configuration with smaller code and faster boot time.

The DSP Collaborative™

The VisualDSP++ environment enables independent third-party companies to add value using ADI's published set of application programming interfaces (API's). The DSP Collaborative is a comprehensive collection of DSP development support companies. The DSP Collaborative product offerings – real-time operating systems, emulators, high-level language compilers, and multiprocessor hardware can interface seamlessly with VisualDSP++ thereby simplifying development across all platforms and targets.

VisualDSP Bundles

Bundle	Suffix	IDE	Debugger	Compiler	Assembler	Linker	Emulation and Simulation Support
Complete Package	FULL	X	X	X	X	X	X
Code Gen Package	CAL			X	X	X	
Assembler Package	AL				X	X	
IDE/Debugger Package	DIS	X	X				X
Floating License	FLOAT	X	X	X	X	X	X

Development Tools
ADSP-2100 Family

Development tools from Analog Devices are one of the industry's most complete lines, from the economical EZ-KIT Lite™ evaluation kits to multiprocessor debuggers. These tools are easy to learn and easy to use, and allow designers to bring DSP-based products to market quickly and efficiently.

VisualDSP Integrated Development Environment

VisualDSP® is a comprehensive toolset for ADSP-218x and ADSP-219x DSPs. VisualDSP enables design engineers to easily develop, debug, and deploy code throughout the research, design, development, and test stages of any project. VisualDSP integrates all of the code generation tools below:

- Assembler
- Linker
- Simulator
- C Compiler
- Debugger
- Librarian
- PROM splitter
- Math, DSP and C runtime library
- Integrated development environment

EZ-KIT Lite™ Evaluation Kit. The EZ-KIT Lite provides an easy way to evaluate the power of ADI's DSPs and begin to develop applications. These systems consist of a stand-alone evaluation board and fundamental debugging software to facilitate architecture evaluations via a PC-hosted tool set. With the EZ-Kit Lite users can:

- Evaluate ADI's DSPs
- Learn about DSP applications
- Simulate & debug applications
- Prototype applications

Emulators. Emulators provide non-intrusive target-based debugging of DSP systems. Compact and easy to use, these in-circuit emulators perform a wide range of emulation functions including single-step and full-speed execution with pre-defined breakpoints, viewing and/or altering of register and memory contents.

Model	Supported DSP
ADDS-2181-EZLITE	ADSP-2100 Family ADSP-2181
ADDS-218X-ICE-1.8V	ADSP-218XM/N Family
ADDS-2189M-EZLITE	ADSP-218XM/N Family
ADDS-2192-12EZLITE	ADSP-2192
VDSP-21XX-PC-FULL	Complete Package ADSP-218x/219x IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support
VDSP-21XX-PC-CAL	Code Gen Package ADSP-218x/219x Compiler, Assembler, Linker
VDSP-21XX-PC-AL	Assembler Package ADSP-218x/219x Assembler, Linker
VDSP-21XX-PC-DIS	IDE/Debugger Package ADSP-218x/219x IDE/Debugger, with Emulation and Simulation Support
VDSP-21XX-PCFLOAT	Floating VisualDSP ADSP-218x/219x
VDSP-21XX-PC-TEST	VisualDSP Test Drive ADSP-218x/219x 30-Day Free Trial
JTAG Emulators for the ADSP-219x DSP Family	
ADDS-APEX-ICE	ADSP-219x
ADDS-SUMMIT-ICE	ADSP-219x
ADDS-TREK-ICE	ADSP-219x
ADDS-MTN-ICE	ADSP-219x

Development Tools
ADSP-21000 SHARC® Family

SHARC® DSPs are the highest performance 32-bit DSPs available. These single-chip system solutions optimize memory, I/O, and core speed. ADI offers over 50 32-bit processors for computing, communications, audio, industrial, mil/aero, and consumer applications.

Within the ADSP-21000 SHARC Family, all processors are code compatible, allowing additional features and performance while protecting software development investment.

The SHARC family is unique among 32-bit DSPs in that it processes fixed-point data at the same speed as it processes floating-point data. Designers may use both math types depending on their application needs.

Development Software

VisualDSP++ is a comprehensive toolset for SHARC DSPs. VisualDSP++ enables design engineers to easily develop, debug, and deploy code throughout the research, design, development, and test stages of any project. VisualDSP++ integrates all of the code generation tools below:

- Assembler
- Linker
- Simulator
- C++ Compiler
- Librarian
- PROM Splitter
- Math, DSP and C++ Runtime Library
- Integrated Development Environment

EZ-KIT Lite™ Evaluation Kit. The EZ-KIT Lite provides an easy way to evaluate the power of ADI's DSPs and begin to develop applications. These systems consist of a standalone evaluation board and fundamental debugging software to facilitate architecture evaluations via a PC-hosted tool set. With the EZ-Kit Lite users can:

- Evaluate ADI's DSPs
- Learn about DSP applications
- Simulate & debug applications
- Prototype applications

Emulators. Emulators provide non-intrusive target-based debugging of DSP systems. Compact and easy to use, these in-circuit emulators perform a wide range of emulation functions including single-step and full-speed execution with pre-defined breakpoints, viewing and/or altering of register and memory contents. DSP emulators are available for PC-AT, PCI, and USB host platforms. Remote emulation and debug is made possible over a local area network with Ethernet-based products.

Model	Supported DSP
ADDS-21061-EZLITE	ADSP-2106X Family
ADDS-21160M-EZLITE	ADSP-21160M/N
ADDS-21161N-EZLITE	ADSP-21161N
ADDS-21065L-EZLITE	ADSP-21065L
VDSP-SHARC-PC-FULL	Complete Package IDE, Debugger, Compiler, Assembler, Linker with Emulation and Simulation Support
VDSP-SHARC-PC-CAL	Code Gen Package Compiler, Assembler, Linker
VDSP-SHARC-PC-AL	Assembler Package Assembler, Linker
VDSP-SHARC-PC-DIS	IDE/Debugger Package IDE/Debugger, with Emulation and Simulation Support
VDSP-SHARC-PCFLOAT	Floating VisualDSP
VDSP-SHARC-PC-TEST	VisualDSP++ Test Drive 30-Day Free Trial
ADDS-APEX-ICE	Apex-ICE USB-Based Emulator
ADDS-TREK-ICE	Trek-ICE Ethernet-Based Emulator
ADDS-SUMMIT-ICE	Summit-ICE PCI-Based Emulator
ADDS-MTN-ICE	Mountain-ICE ISA-Based Emulator

http://www.analog.com/dsp/tools

The DSP Collaborative™
ADI's Third Party Partner Program

Tap Into the Experience and Global Reach of the DSP Collaborative

Working together to extend your design team

The DSP Collaborative partners (Analog Devices' Third Party Program) offer tools, services and solutions for a wide range of applications/markets:

- Communications
- Audio
- Medical Imaging
- Radar/Sonar
- Motion Control
- Motor Control
- Industrial Automation
- Signal Intelligence

When you select Analog Devices as your DSP vendor, you're broadening your design team to include the industry-leading resources of the DSP Collaborative. The DSP Collaborative is comprised of over 80 partners who offer more than 400 commercial products, in addition to hundreds of custom solutions that build on more than 30 years of signal processing experience found in every one of our DSPs. These partners offer consulting services as well as a wide range of commercial off-the-shelf (COTS) products. Their development tools are specifically designed to work with Analog Devices' DSP-based systems.

With the DSP Collaborative, you are supported by highly-reputable brands, patented technologies, and the pioneers in real-time system design and debug. The DSP Collaborative partners offer products and services that provide both system and application-level expertise.

Speed up your design process by leveraging the solutions our partners have to offer:

- Debuggers
- Real-Time Operating Systems
- Development and Evaluation Boards
- MATLAB® DSP Support
- Algorithms and Libraries
- Emulators
- DSP Systems
- COTS Hardware Boards

Design with Analog Devices' DSP Collaborative team approach with a proven strategy for maximizing your resources!

http://www.analog.com/dsp/3rdparty

DSP Competitor Cross Reference Guide

Device Part Number	ADI Suggested Functional Replacement Device	Number of Cores	MMACS	RAM (Kwords)	Operating Voltage (Core, I/O)	Smallest Package
Analog Devices 218x Family						
ADSP-2181		1	40	32	5V	128TQFP
ADSP-2183		1	52	32	3.3V	128TQFP
ADSP-2184		1	40	8	5V	100TQFP
ADSP-2185		1	33	32	5V	100TQFP
ADSP-2186		1	40	16	5V	144BGA*
ADSP-2184L		1	40	8	3.3V	144BGA*
ADSP-2185L		1	52	32	3.3V	144BGA*
ADSP-2186L		1	40	16	3.3V	144BGA*
ADSP-2187L		1	52	64	3,3V	144BGA*
ADSP-2185M		1	75	32	2.5V, 2.5V-3.3V	144BGA*
ADSP-2186M		1	75	16	2.5V, 2.5V-3.3V	144BGA*
ADSP-2188M		1	75	104	2.5V, 2.5V-3.3V	144BGA*
ADSP-2189M		1	75	80	2.5V, 2.5V-3.3V	144BGA*
ADSP-2184N		1	80	8	1.8V/3.3V	144BGA*
ADSP-2185N		1	80	32	1.8V/3.3V	144BGA*
ADSP-2186N		1	80	16	1.8V/3.3V	144BGA*
ADSP-2187N		1	80	64	1.8V/3.3V	144BGA*
ADSP-2188N		1	80	104	1.8V/3.3V	144BGA*
ADSP-2189N		1	80	80	1.8V/3.3V	144BGA*
ADSP-2192		2	320	132	2.5V/3.3V	144LQFP
Texas Instruments C54X Family						
TMS320C541	ADSP-2181, 2185	1	40	5	5V	100TQFP
TMS320C542	ADSP-2181, 2185	1	40	10	5V	128TQFP
TMS320LC541	ADSP-2185L, 2186L	1	66	5	3.3V	100TQFP
TMS320LC542	ADSP-2185L, 2186L	1	50	10	3.3V	128TQFP
TMS320LC543	ADSP-2185L, 2186L	1	50	10	3.3V	100TQFP
TMS320LC545A	ADSP-2185L, 2186L	1	66	6	3.3V	128TQFP
TMS320LC546A	ADSP-2185L, 2186L	1	66	6	3.3V	100TQFP
TMS320LC548	ADSP-2185L, 2187L	1	66	32	3.3V	144BGA*
TMS320LC549	ADSP-2185L, 2187L	1	80	32	3.3V	144BGA*
TMS320UC5402	ADSP-2186N	1	80	16	1.8V, 1.8V-3.3V	144BGA*
TMS320UC5409	ADSP-2185N	1	80	32	1.8V, 1.8V-3.3V	144BGA*
TMS320UVC5401	ADSP-2184N	1	50	8	1.8V, 3.3V	144BGA*
TMS320UVC5402	ADSP-2186N	1	30	16	1.2V, 1.2V-2.75V	144BGA*
TMS320UVC5409	ADSP-2185N	1	30	32	1.2V, 1.2V-2.75V	144BGA*
TMS320VC549	ADSP-2185N	1	120	32	2.5V, 3.3V	144BGA*
TMS320VC5402	ADSP-2186N	1	100	16	1.8V, 3.3V	144BGA*
TMS320VC5409A	ADSP-2185N	1	160	32	1.8V, 3.3V	144BGA*
TMS320VC5410A	ADSP-2187N	1	160	64	2.5V, 3.3V	176BGA
TMS320VC5416	ADSP-2188N	1	160	128	1.5V, 3.3V	144BGA*
TMS320VC5420	ADSP-2188N	2	200	200	1.8V, 3.3V	144BGA*
TMS320VC5421	ADSP-2192	2	200	256	1.8V, 3.3V	144BGA*
TMS320VC5441	ADSP-2192	4	532	640	1.5V, 3.3V	179BGA
TMS320VC5510	ADSP-219x	1	400	160	1.6V, 3.3V	240BGA
Texas Instruments C62X Family						
TMS3206201	ADSP-2192	1	400	80	1.8V, 3.3V	352BGA
TMS3206202	ADSP-2192	1	500	128	1.8V, 3.3V	352BGA
TMS3206203	ADSP-2192	1	600	608	1.5V, 3.3V	352BGA
TMS3206204	ADSP-2192	1	400	80	1.5V, 3.3V	288BGA
TMS3206205	ADSP-2192	1	400	80	1.5V, 3.3V	288BGA
TMS3206211	ADSP-2192	1	334	72	1.8V, 3.3V	256BGA

* Note: Analog Devices' BGA package is 10 mm x 10 mm – TI BGA package is 12 mm x 12 mm

Benchmarks
Comparing DSPs

To truly assess a processor's performance, you have to look beyond MHz, MIPS, or MFLOPS. There are many attributes which may be more accurate predictors of a DSP's real-time embedded processing performance.

Circular Buffers

Circular buffers allow a region of memory to be continually accessed without explicit program interaction. The buffer uses a pointer that automatically resets to the beginning of the buffer (wrap around) if the pointer is advanced beyond the last location in the buffer. Circular buffers are a key feature of DSP routines. Multiple buffers are used in the same routine to store filter coefficients and implement a delay line of input samples. Performance suffers if the DSP core has to perform pointer calculations along with the calculations for the routine. Performance also suffers if the DSP core only supports one circular buffer and must save and restore address registers to implement multiple buffers.

ADI's DSPs have hardware support for multiple circular buffers, eliminating processor overhead for address calculations.

Data Registers

The number of general-purpose data registers available can impact the code performance. Fewer registers require intermediate results to be stored in memory decreasing performance and increasing the load on the memory bus.

ADI DSPs feature a secondary register set which allows for quick context saves when interrupts occur, rather than delaying responses to the interrupt while all register values are saved to memory.

DMA Channels/Non-Intrusive DMA

The DMA (Direct Memory Access) channels transfer data between an external source and the DSP's on-chip memory. With DMA channels, data transfers occur without the core processor having to execute data movement instructions. For example, the overhead clock cycles used to move data for an FFT can add a significant amount of time to overall algorithm execution. With multiple DMA channels available, all data transfers happen without core involvement, eliminating any overhead clock cycles.

One of the strengths of Analog Devices' DSP architecture is that these DMAs do not interfere with the core operation. This capability is referred to as non-intrusive or zero-overhead DMA.

Interrupt Latency

Interrupt latency is a measure of how quickly a DSP responds to an interrupt. Quick response is important especially in real-time processing. For example, an interrupt might indicate the availability of data which is only available for a finite amount of time. Therefore, fast response is critical or the data will be lost.

ADI DSPs feature fast interrupt response time for quick execution of interrupt service routines.

Benchmarks

Multiprocessing Support

Even with the powerful DSPs available today, there are times when the DSP task for a given system does not fit into a single DSP. Examples of such applications include sonar, radar, medical imaging, audio mixers, etc. In these cases, the ability to connect multiple DSPs in a system without any glue logic greatly simplifies the implementation.

ADI offers SHARC DSPs with specialized hardware for glueless multiprocessing.

On-Chip Memory/On-Chip SRAM Size

The amount of on-chip memory available can greatly impact system performance, cost, size, power consumption and complexity. Any time the DSP core accesses external memory, the performance can suffer. Off-chip memory often requires the core to wait additional cycles. In contrast, the DSP core can access on-chip memory at the same rate as its instruction rate. The addition of external memory adds extra components to the system which increases cost, power consumption, and complexity.

ADI leads the industry in DSP SRAM integration. ADI processors have on-chip memories which often eliminate the need for external memory in a system. Furthermore, the memory is configurable for data word size, code word size and storage size. This allows designers to tailor the memory to meet the algorithm requirements.

TDM Mode

TDM (Time Division Multiplexed) mode refers to time division multiplexing which is a common mode for transferring serial data. In telecommunications applications, T1 and E1 lines use TDM. TDM allows multiple serial devices to send and receive information using the same physical connection. TDM also allows communication between multiple DSPs.

All ADI DSPs support TDM mode in the serial ports.

Zero-Overhead Looping

The code for most DSP routines falls naturally into a set of nested loops. Without the support for zero-overhead looping, the DSP core must spend cycles calculating the loop termination values, in addition to the cycles used to process the algorithm's computations. Without zero-overhead looping, performance degrades.

ADI offers 16-bit fixed point and 32-bit fixed/floating point DSPs with zero overhead, nestable looping to save instruction cycles.

ADSP-2100 Family Benchmarks
16-Bit DSPs

The flexibility and power of the ADSP-2100 Family provides users with:

- Best price/performance over a wide range of applications due to flexible architecture and high level of memory and peripheral integration
- Fastest interrupt response time due to alternate register set
- High dynamic range offered by 40-bit accumulator
- Easy to use assembly language syntax

ADSP-218x Family	
Single Sample FIR Filter	31 Inst. Clock
Complex Block FIR Filter	2941 Inst. Clocks
IIR Biquad Filter Section	7 Inst. Clocks
Lattice Filter Section	5 Inst. Clocks
256-Point Complex FFT	7372 Inst. Clocks
1024-Point Complex FFT	34K Inst. Clocks
4096-Point Complex FFT	149K Inst. Clocks
256-Tap LMS Adaptive Filter Coefficient Update	516 Inst. Clocks
10th Order LPC Analysis (240-Point Rectangular Window)	4666 Inst. Clocks
ADPCM-Full Transcode (CCITT G.721, ANSI TI, 301-1987)	893 Inst. Clocks

Benchmarks for ADSP-218X DSPs

Modem Algorithm	MIPS	PM	DM	Comments
V.34 Annex 12	23	16K	16K	@33.6 Kbps
V.34	20	16K	16K	
V.32bis	11.5	7.5K	7K	
V.22bis	3.4	5.2K	1.1K	
V.42	0.5	5.3K	3.8K	@28.8 Kbps
V.42bis	4.5	1K	3.7K	@28.8 Kbps (512 entries)
MNP2-5	3.5	4.3K	2K	
V.17 Fax (Group3)	6.5	7.7K	2.5K	
T.30/T.4 Fax Protocol	2.5	7.6K	8.9K	
G.729 Annex A	10	7K	3K	

Speech Algorithm	O/P Rate	MIPS	PM	DM
G.711	64 Kbps	0	0	0
G.721	32 Kbps	7.6	628	137
G.726	16-40 Kbps	7.5	<1K	<200
G.722	64 Kbps	12.4	1312	208
G.723	5.3/6.3 Kbps	20	8.2K	12.5K
G.728	16 Kbps	28	7.2K	2K
G.729A	8 Kbps	17	9.6K	5K
G.729A	8 Kbps	10.8	7.5K	2K
G.729	8 Kbps	21	10.2K	5.4K
GSM-FR	13 Kbps	3.3	<2K	<1K
GSM-EFR	12.2 Kbps	18.5	10.5K	4K
GSM-HR	5.6 Kbps	23	14K	7K
M-GSM	5.0 and 6.5 Kbps	9	<2K	<1K
CELP	4.3 and 7.5 Kbps	12.5	1.5K	1.5K

ADSP-21000 SHARC® Family Benchmarks
32-Bit DSPs

Just looking at the cycle time, clock speed, MIPS or MFLOPS of a DSP cannot give an accurate indication of the true performance of the processor. Benchmarks are important in that they show how a particular DSP performs in the context of an application. The smaller the benchmark number, the quicker the algorithm execution. If a DSP can perform the task quicker, the processor can perform more tasks in a given amount of time.

SHARC DSPs are the highest performance 32-bit DSPs available. These processors excel at IEEE floating-point math, 32-bit fixed-point math, and extended precision 40-bit floating point.

The ADSP-21000 Family offers a maximum performance for minimum system cost, while dramatically shortening product development time and critical time-to-market.

	ADSP-21065L	ADSP-21161N
Clock Speed	66 MHz	100 MHz
Instruction Cycle Time	15 ns	10 ns
MFLOPS Sustained, Peak	132, 198 MFLOPS	400, 600 MFLOPS
MOPS (32-bit Fixed-Point) Sustained, Peak	132, 198 MFLOPS	400, 600 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	0.27 ms (SISD)	0.09 ms (SIMD)
FIR Filter (per Tap)	15 ns	10 ns
IIR Filter (per Biquad)	60 ns	10 ns
Matrix Multiply (3x3) x (3x1) (4x4) x (4x1)	 135 ns 240 ns	 56.25 ns 80 ns
Divide (y/x)	90 ns	30 ns
Inverse Square Root	135 ns	45 ns

1024-Point Complex FFT (in place)
32-BIT Floating-Point DSPs

DSP Processor	Instruction Rate	Instruction Cycle Time	Number of Cycles	Total FFT Time
TMS320C6701	167 MHz	6 ns	19, 875	0.12 ms
TMS320C6711	150 MHz	6.7 ns	19, 875	0.13 ms
TMS320C6712	100 MHz	10 ns	19, 875	0.19 ms
ADSP-21065L	66 MHz	15 ns	18, 221	0.27 ms
ADSP-21160N	90 MHz	11 ns	9, 111	0.10 ms
ADSP-21161N	100 MHz	10 ns	9, 111	0.09 ms

Specification Source:
TI website www.ti.com

Part Numbering System

DSP Part Numbering

Analog Devices Digital Signal Processing

Power Code
L = Low Power (3.3V)
M = 2.5V internal (3.3V I/O)
No Suffix = 5V
Exception: ADSP-2183 = 3.3V

Packaging Code
S = Plastic Quad Flat Pack (MQFP)
ST = Thin LQFP
B = Plastic Ball Grid Array (PBGA)
Z = Ceramic QFP, Heat slug up
W = Ceramic QFP, Heat slug down
P = PLCC
G = PGA
CA = mini BGA

X-Grade
X = X-Grade
No Suffix = Production Released

ADSP-21xx(x) X X XX-### XR or REEL

Product Number
-21XX = 16 Bit
-21XXX = 32 Bit

Temperature Codes
K = Commercial
0ºC to 70ºC ambient – 16 Bit
0ºC to 85ºC case – 32 Bit
T = Extended temperature grades
A = Industrial: -40ºC to 85ºC case
B = Industrial: -40ºC to 85ºC ambient
C = Industrial: -40ºC to 100ºC case

Speed Grade Code
Speed Grade = 4* MIPS (or MHz)
e.g.: -133 = 33 MIPS = 40 MHz
-160 = 40 MIPS = 40 MHz
-200 = 50 MIPS = 50 MHz
-300 = 75 MIPS = 75 MHz
Exception: ADSP-2116x products
Speed Grade = 1* MIPS (or MHz)
e.g.: -100 = 100 MIPS = 100 MHz

Tape and Reel

ADSP-219X Part Numbering

x - Device Type
Multi-Channel
1 = 65K
2 = 128K
3 =
4 =
Single Channel
5 =
6 = 16K
7 =
8 =

y - Peripherals
A = Set 1
B = Set 2
C = :
D = :

F = Flash

v - Voltage
M = 2.5
N = 1.8
P =1.5
R = 1.2
S = 1.0

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	D	S	P	-	2	1	9	x	y	-	v	t	p	p	q	q	q
								1	A		M	K	S	T			
								2	B		N	B	C	A			
								3	C		P	Y					
								4	D		R	S					
								5			S						
								6	F								
								7									
								8									

q - Speed
100 = 100 MHz

p - Package
ST - LQFP
CA - MiniBGA

t - Temp
K = 0/+70
B = -40/+85
Y = -40/+105
S = -55/+125

A	D	S	P
2	1	x	x
		9	x

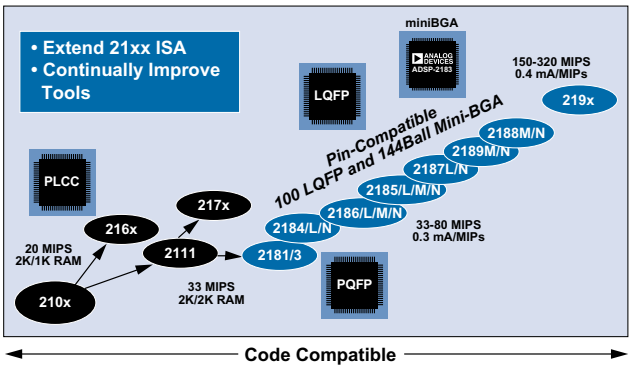
Analog Devices DSP
16-Bit fixed-point code compatible DSPs
Integrates 9x core

Processor Selection Guide
ADSP-2100 16-Bit DSP Family

The ADSP-2100 family is built around a common instruction set architecture (ISA) which is optimized for signal processing. Within the ADSP-2100 family, all processors are code compatible, allowing additional features and performance while protecting software development investment. Each family member differs in circuitry added to the base architecture such as memory, processor speed, serial ports and other peripherals. The following pages detail the ADSP-218x and ADSP-219x DSPs, the newest processors in the ADSP-2100 family.

16-Bit DSP Family Tree

A History of Improvements in **Packaging • Power • Performance**



16-BIT Generic	Package	Max MIPs	Vcc	Program RAM Words	Program ROM Words	Data RAM Words	Serial Ports	Price**
ADSP-2192	ST	320	2.5V	32K		100K	0	$60.00
ADSP-2188M	ST, CA	75	2.5V	48K		56K	2	$32.00
ADSP-2188N	ST, CA	80	1.8V	48K		56K	2	$30.00
ADSP-2189M	ST, CA	75	2.5V	32K		48K	2	$26.50
ADSP-2189N	ST, CA	80	1.8V	32K		48K	2	$25.00
ADSP-2187L	ST	52	3.3V	32K		32K	2	$37.17
ADSP-2187N	ST, CA	80	1.8V	32K		32K	2	$20.00
ADSP-2185	ST	33	5V	16K		16K	2	$23.05
ADSP-2185L	ST, CA	52	3.3V	16K		16K	2	$21.95
ADSP-2185M	ST, CA	75	2.5V	16K		16K	2	$11.50
ADSP-2185N	ST, CA	80	1.8V	16K		16K	2	$11.25
ADSP-2186	ST, CA	40	5V	8K		8K	2	$17.28
ADSP-2186L	ST, CA	40	3.3V	8K		8K	2	$17.28
ADSP-2186M	ST, CA	75	2.5V	8K		8K	2	$9.00
ADSP-2186N	ST, CA	80	1.8V	8K		8K	2	$8.50
ADSP-2184	ST	40	5V	4K		4K	2	$10.00
ADSP-2184L	ST	40	3.3V	4K		4K	2	$10.00
ADSP-2184N	ST, CA	80	1.8V	4K		4K	2	$7.00
ADSP-2183	S, CA	52	3.3V	16K		16K	2	$21.95
ADSP-2181	S, ST	40	5V	16K		16K	2	$20.95
ADSP-2173	S, ST	20	3.3V	2K		2K	2	$45.13
ADSP-2171	S, ST	33	5V	2K		2K	2	$37.41
ADSP-2166	P, S	16.7	3.3V	1K	12K	4K	2	CF*
ADSP-2165	P, S	20	5V	1K	12K	4K	2	CF*
ADSP-2164	P, S	10.2	3.3V		4K	0.5K	2	CF*
ADSP-2163	P, S	16.7	5V		4K	0.5K	2	CF*
ADSP-2162	P, S	10.2	3.3V		8K	0.5K	2	CF*
ADSP-2161	P, S	16.7	5V		8K	0.5K	2	CF*
ADSP-2115	P, S, ST	25	5V	1K		0.5K	2	$14.11
ADSP-2111	G, S	20	5V	2K		1K	2	$114.06
ADSP-2105	P	20	5V	1K		0.5K	1	$11.90
ADSP-2104	P	20	5V	0.5K		0.25K	1	$7.32
ADSP-2103	P, S	10	3.3V	2K		1K	2	$26.02
ADSP-2101	G, P, S	25	5V	2K		1K	2	$21.70

Package: B = Plastic Ball Grid Array (PBGA)
G = Ceramic Pin Grid Array (PGA)
P = Plastic Leaded Chip Carrier (PLCC)
S = Plastic Quad Flat Pack (PQFP)
ST = Thin Quad Flat Pack (LQFP)
CA = Mini Ball Grid Array

* Contact factory for pricing
** US Dollars. Lowest grade suggested resale price per unit in 100 unit quantities

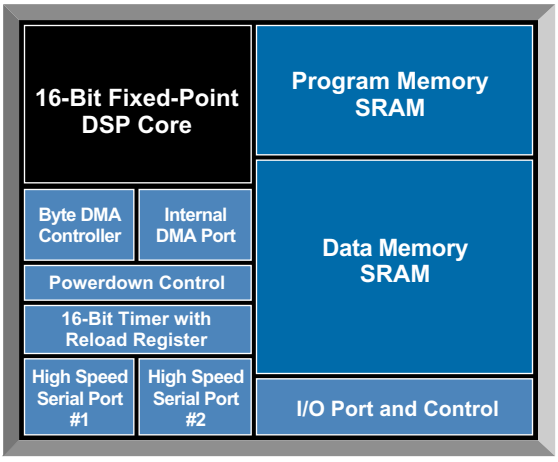
"M" and "N" Series Pin Compatibility
Mitigates Design Risks

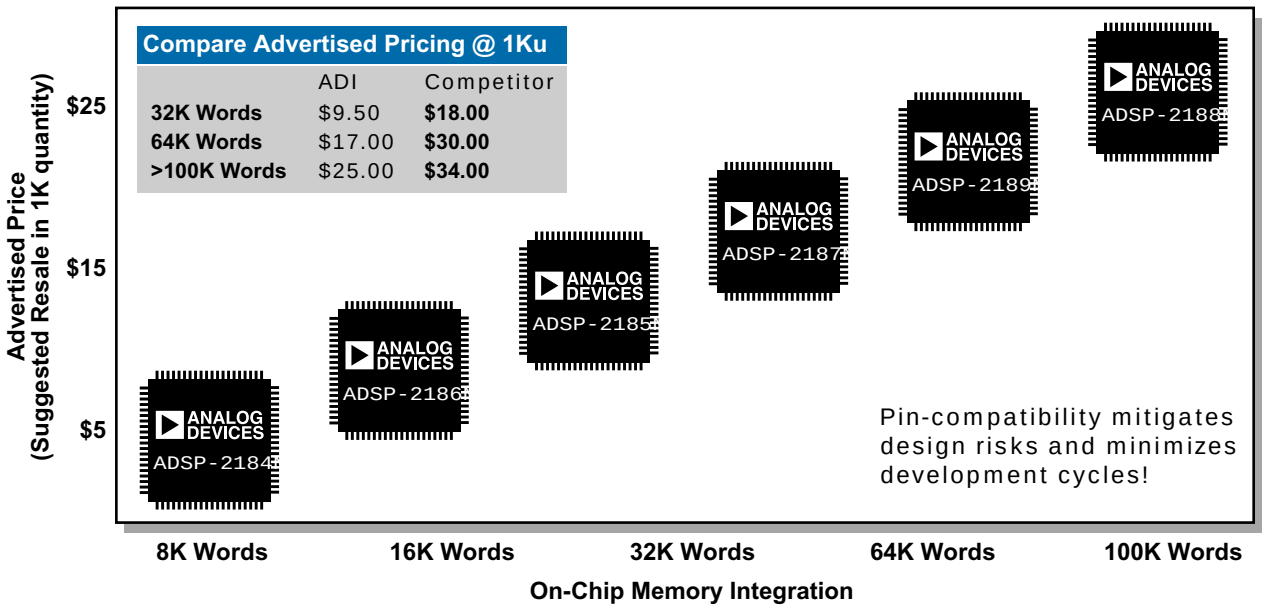
Analog Devices' industry-leading DSP and SRAM integration capability is evident in the ADSP-218x family. Well known for the 32-bit DSP and SRAM integration pioneered in the SHARC® family, Analog Devices provides the 16-bit complement in the ADSP-218x family. With up to 2 Mbits of on-chip SRAM, many functions run without the need for external memory, vastly simplifying the board design, algorithm development and debug process. In addition to minimizing memory I/O bottlenecks, executing algorithms using on-chip memory reduces chip count, system cost, board space, and power consumption. Large amounts of SRAM, coupled with the ADSP-2100 family's sophisticated DMA and programming features, make the ADSP-218x processors the best choice to make your design challenge easier.

Packaging technology also plays an important role in how easily designers can incorporate these processors into their applications. Advanced miniaturization techniques and pin-out standardization can significantly simplify the design-in process.

The ADSP-2188N, for example, is packaged in a tiny 10mm x 10mm Ball Grid Array (mini BGA). In a one-centimeter-square package, the design engineer has 80 MIPS, 2 Mbits of SRAM, and two serial ports.

Likewise, Analog Devices' pin-for-pin compatible packaging strategy saves designers time. With little or no change to the hardware, designers can migrate to higher speeds, lower voltages, and larger memory sizes.





ADSP-218x Family

Code-and Pin-Compatible Family of 16-Bit, Fixed Point DSPs

Features

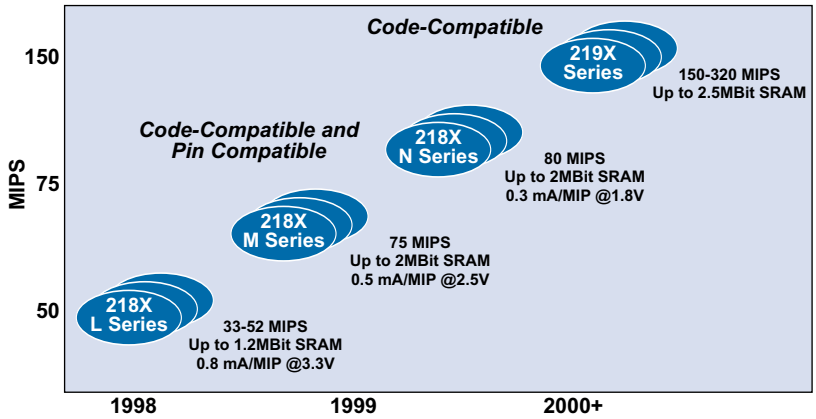
- Easy to use algebraic-like assembly language syntax
  - – All instructions execute in a single cycle
  - – Over 100 pin and code compatible devices
  - – Fast interrupt response
- 160 Kbits to 2 Mbits of on-chip SRAM
- DSP balanced for data processing and data I/O
  - – Multifunction instructions allow simultaneous operations of:
    - Computational units
    - 2 data address generators
    - Powerful program sequencer
  - – Byte DMA transfers up to 4Mbytes of stored code or data
  - – 2 Serial ports, including multi-channel serial port for direct interfacing to T1/E1 lines
  - – 16-Bit wide internal DMA port
- As low as .3 mA/MIP at 80 MHz
- 28 to 80 MHz
- 5V/3.3V/2.5V/1.8V Supply Voltages

Benefits

- Greater flexibility in system design because of performance and memory options in the same package type
- Large amounts of on-chip SRAM eliminate the need for external memory thus simplifying algorithm development and reducing chip count, board space and power consumption
- Several types of peripheral DMA support allow for modular system designs with a minimum of external circuitry
- Multi-function instructions and zero overhead nested looping capabilities combine to produce efficient algorithm execution

Applications

- Consumer Telephony
- Cellular Accessories
- Embedded Speech Processing
- POS Terminals
- Smartcard Readers
- PBX
- Portable Text Scanners
- Audio Equipment
- Multi-channel Voice
- Data Encryption
- ISDN Modems
- Global Positioning
- Navigation



ADSP-218x "N" Series
Low Power ADSP-218x Family

The new ADSP-218x "**N**" series is a low power (1.8V) 16-Bit DSP family that is pin compatible with all the ADSP-218xM products and code compatible with all ADSP-21xx DSPs.

Features

- 0.3 mA/MIP @ 1.8 volt core supply
- 12.5 ns instruction cycle time (80 MIPS)
- Up to 48K words of on-chip program RAM
- Up to 56K words of on-chip data memory RAM
- I/O voltage support to 3.3 volts
- 16-Bit Internal DMA Port
- 8-Bit Byte Memory DMA
- Two Double Buffered Serial Ports (1 with TDM mode)
- I/O Memory Interface w/2048 Locations
- ADSP-2100 Family code & function compatible
- 100-Lead LQFP, 144-Lead mini-BGA

Benefits

- Simple algebraic assembly language reduces development time and time-to-market
- Pin-compatible packages mitigates product development risks
- 16-Bit DMA port makes bus interfacing easier
- Code compatible with all 21xx derivatives ensures re-use of legacy code
- Large on-chip memory eliminates the need for expensive SRAM
- 144 Ball mini-BGA package provides for maximum space savings (10 mm x 10 mm)

Applications

- Consumer Telephony
- Embedded Speech Processing
- POS Terminals
- PBX
- Smartcard Readers
- Multi-channel Voice Processing
- Satellite Telephone
- Industrial Measurement & Control
- Data Encryption
- ISDN Modems
- VOIP Phone
- Global Positioning
- Internet Gateway

Development Tools	
ADDS-218x-WKSHP	DSP Workshop
ADDS-218x-ICE-1.8V	In-circuit Emulator
ADDS-2189M-EZ-LITE	Evaluation Kit
VDSP-21xx-PC-FULL	Complete Software Pkg

Model	PM/DM	MHz	Temperature	Pin/Pkg	Price (100-499)**
ADSP-2184NBST-320*	4K/4K	80	-40ºC to +85ºC	128-LQFP	$7.00
ADSP-2184NBCA-320	4K/4K	80	-40ºC to +85ºC	144-MBGA	$9.00
ADSP-2186NBST-320	8K/8K	80	-40ºC to +85ºC	128-LQFP	$8.50
ADSP-2186NBCA-320	8K/8K	80	-40ºC to +85ºC	144-MBGA	$10.50
ADSP-2185NBST-320	16K/16K	80	-40ºC to +85ºC	128-LQFP	$11.25
ADSP-2185NBCA-320	16K/16K	80	-40ºC to +85ºC	144-MBGA	$13.50
ADSP-2187NBST-320	32K/32K	80	-40ºC to +85ºC	128-LQFP	$20.00
ADSP-2187NBCA-320	32K/32K	80	-40ºC to +85ºC	144-MBGA	$22.00
ADSP-2189NBST-320	32K/48K	80	-40ºC to +85ºC	128-LQFP	$25.00
ADSP-2189NBCA-320	32K/48K	80	-40ºC to +85ºC	144-MBGA	$27.00
ADSP-2188NBST-320	48K/56K	80	-40ºC to +85ºC	128-LQFP	$30.00
ADSP-2188NBCA-320	48K/56K	80	-40ºC to +85ºC	144-MBGA	$32.00

* N indicates 1.8V core supply
** Budgetary pricing – subject to change

ADSP-218x "M" Series
The Compatible DSP Family

The ADSP-218x "**M**" Series expands the code-compatible, pin-compatible portfolio; offers the highest performance and memory integration at 2.5V, and is code compatible with all ADSP-21xx DSPs.

Features

- 13 ns instruction cycle time (75 MIPS)
- Up to 48K words of on-chip program RAM
- Up to 56K words of on-chip data memory RAM
- 2.5 volt core supply with up to 3.3 volt I/O
- 16-Bit Internal DMA Port
- 8-Bit Byte Memory DMA
- Two Double Buffered Serial Ports (1 with TDM mode)
- I/O Memory Interface w/2048 Locations
- ADSP-2100 Family code & function compatible
- 0.5 mA/MIP power consumption
- 100-Lead LQFP, 144-Lead miniBGA

Benefits

- Algebraic assembly language for easy programming
- On-chip RAM and 6 DMA channels
- 16-Bit DMA port makes bus interfacing easier
- 5 sleep and powerdown modes maximize battery life
- 144 Ball mini-BGA package provides for maximum space savings (10 mm x 10 mm)

Applications

- Consumer Telephony
- Embedded Speech Processing
- POS Terminals
- PBX
- Smartcard Readers
- Multi-channel Voice Processing
- Satellite Telephone
- Industrial Measurement and Control
- Zero Install Full Duplex Hands Free Car Kit
- Speaker Phones
- Digital Speech Interpolation
- Data Encryption
- ISDN Modems
- VOIP Phone
- Pattern Matching
- Global Positioning
- Navigation
- Network Access Servers

Development Tools	
ADDS-218x-WKSHP	DSP Workshop
ADDS-218x-ICE-1.8V	In-circuit Emulator
ADDS-2189M-EZ-LITE	Evaluation Kit
VDSP-21xx-PC-FULL	Complete Software Pkg

Model	PM/DM	MHz	Temperature	Pin/Pkg	Price (100-499)
ADSP-2186MKST-300*	8K/8K	75	0ºC to 70ºC	128-LQFP	$9.00
ADSP-2186MBST-266	8K/8K	66	-40ºC to +85ºC	128-LQFP	$9.00
ADSP-2186MKCA-300	8K/8K	75	0ºC to 70ºC	144-MBGA	$11.00
ADSP-2186MBCA-266	8K/8K	66	-40ºC to +85ºC	144-MBGA	$11.00
ADSP-2185MKST-300	16K/16K	75	0ºC to 70ºC	128-LQFP	$11.50
ADSP-2185MBST-266	16K/16K	66	-40ºC to +85ºC	128-LQFP	$11.50
ADSP-2185MKCA-300	16K/16K	75	0ºC to 70ºC	144-MBGA	$13.50
ADSP-2185MBCA-266	16K/16K	66	-40ºC to +85ºC	144-MBGA	$13.50
ADSP-2189MKST-300	32K/48K	75	0ºC to 70ºC	128-LQFP	$26.50
ADSP-2189MBST-266	32K/48K	66	-40ºC to +85ºC	128-LQFP	$26.50
ADSP-2189MKCA-300	32K/48K	75	0ºC to 70ºC	144-MBGA	$28.50
ADSP-2189MBCA-266	32K/48K	66	-40ºC to +85ºC	144-MBGA	$28.50
ADSP-2188MKST-300	48K/56K	75	0ºC to 70ºC	128-LQFP	$32.00
ADSP-2188MBST-266	48K/56K	66	-40ºC to +85ºC	128-LQFP	$32.00
ADSP-2188MKCA-300	48K/56K	75	0ºC to 70ºC	144-MBGA	$34.00
ADSP-2188MBCA-266	48K/56K	66	-40ºC to +85ºC	144-MBGA	$34.00

* M indicates 2.5V operation

ADSP-219x Family
Code Compatible, Low Cost, Low Power

The ADSP-219x family maintains code compatibility with the ADSP-218x while extending architectural performance to beyond 300 MIPS. Streamlined for faster processing and improved C-compiler efficiency, with power consumption better than 0.4mA/MIP, the ADSP-219x family will include multiple DSPs for applications such as telephony, industrial equipment, automotive, and consumer electronics. JTAG support is also included to provide a more robust software emulation and test capability.

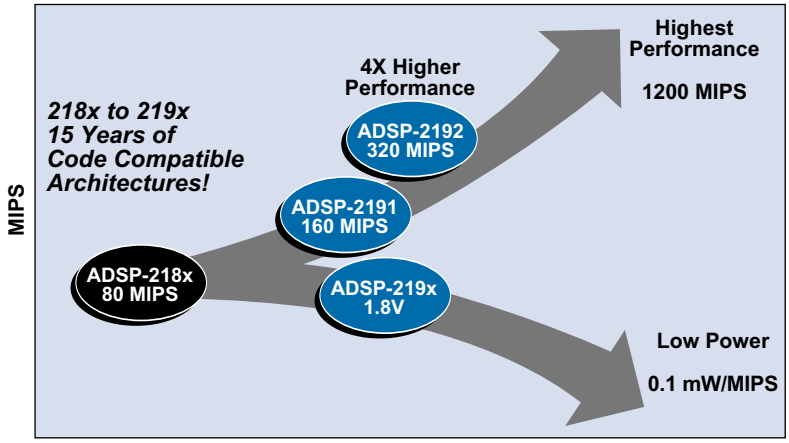
Processor Core

Based on the industry-proven ADSP-21xx architecture, the ADSP-219x core architecture consists of three computational units, data registers, program sequencer, and two data address generators.

Computational capabilities include an Arithmetic Logic Unit (ALU), a Multiply-Accumulator (MAC) with 40-bit precision, and a general purpose, 32-bit wide barrel shifter. Any data register in the 32-register register-file can be used as an input to any computational unit.

This mathematical capability is fed by two powerful data address generators that can operate simultaneously, enabling dual data operands in a single-cycle. Data can be accessed anywhere in a 16 Mword space through the address generators' 16-bit base register set and 8-bit page registers. A flexible set of addressing modes allows for efficient data transfers and stack manipulation.

Instruction flow is handled through an efficient Program Sequencer that ensures single-cycle operation for all mathematical operations. A selective instruction provides high-speed operation and power efficiency without sacrificing intuitive operation and easy programmability.



Compiler-Friendly

Many of the enhancements in the ADSP-219x architecture are designed to improve compiler efficiency. A global register allocator and support for register-file-like computations reduce spills and reduce reliance on the local stack. The compiler features DSP intrinsic support including fractional and complex math.

Some of the enhancements to the ADSP-219x core to improve C compiler efficiency are: more flexible addressing modes in DAG registers, register file capable instructions, added depth to stacks, added secondary DAG registers and extended address reach to 16 Mwords.

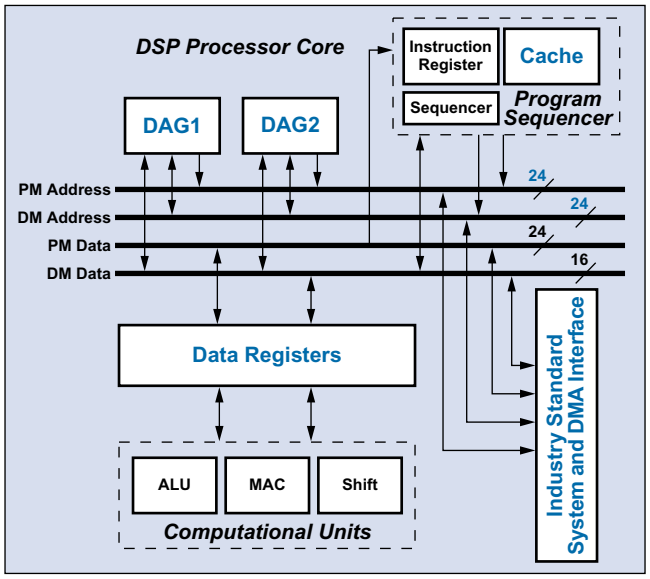
Extended Address Reach

The address reach has been extended to 24-bits. This supports 64 Kword direct memory addressing or 16 Mword paged memory addressing. All existing addressing modes are supported and five new DAG addressing modes have been added.

The addressing modes include:

- Direct (immediate address) to/from a register in groups 0-3
- Indirect post-modify to/from a DREG
- Indirect post-modify write with immediate data
- Two indirect post-modify reads to AX/AY/MX/MY only
- Modify address register (without a transfer)
- Indirect post-modify to/from any register in banks 0-3
- Indirect post-modify with immediate 8-bit offset
- Indirect with immediate 8-bit offset to/from any DREG
- Indirect with M-register offset to/from any register
- Modify address register immediate (2's complement modifier)

The development tools are VisualDSP++ compatible, supporting a unified ADSP-2100 and SHARC DSP development environment. Designers work with the same tool chain across all Analog Devices' DSPs.



- Compiler-efficient data register design
- Program sequencer for fast code execution
- Fully transparent instruction cache for dual operand fetches

ADSP-219x Core Block Diagram

ADSP-2192
First ADSP-219x Family Member

The ADSP-2192 is a dual-core 16-bit fixed point DSP, code compatible with the popular ADSP-218x family and the first member of the ADSP-219x DSP Family – available now. The ADSP-2192 combines two ADSP-219x cores with industry standard PCI, USB and AC-97 glueless system interfaces. This reduces overall system cost and OEM development time.

Features

- 160 MHz/320 MIPs High-performance Dual Core, 16-bit Device
- 2.4 Mbits On-chip SRAM
- PCI 2.2 33MHz/32-bit Compliant
- Integrated USB 1.1 Compliant Interface
- AC '97 Rev 2.1 Compliant Interface
- On-chip Boot ROM
- 8 Dedicated General Purpose I/O Pins
- 14 DMA Channels
- Supported by ADI's VisualDSP Integrated Development Environment
- Supported by an Optimizing C Compiler
- 2.5 volt supply with 3.3 volt I/O
- 144-Lead LQFP

Applications

- Integrated Access Devices (IAD)
- SOHO Telephony
- Data Acquisition
- Multi-mode Modems
- Voice/Fax Over IP
- Voice Over ATM
- Voice Mail Systems
- PBX Extenders
- Echo Cancellation

Benefits

- Dual-core, device provides more flexibility and higher sustained performance
- Large on-chip memory reduces off-chip memory access bottlenecks and overall system cost
- Unified memory space allows more efficient use of memory
- Efficient C Compiler for ease of programming

Model	MHZ	Pin/Pkg	Price** (100-499)
ADSP219212MKST160x*	320	144-LQFP	$60.00

Commercial Temp (0ºC to 70ºC)
* M Indicates 2.5 Volt Operation
** Budgetary pricing – subject to change

Development Tools	
ADDS-219X-WKSHP	DSP Workshop
ADDS-219X-EZ-ICE	In-circuit Emulator
ADDS-2192-12EZLITE	Evaluation Kit
VDSP-21XX-PC-FULL	Complete SW Pkg

ADSP-2192 Assembly Benchmarks

Algorithm	Description	Average Cycle Time (µs)[1,2]
1024 Point Complex FFT (Radix 2 with reversal)	Complex 1024-point Decimation-in-Time FFT on a complex, normally ordered, input. The original complex input is destroyed in the process. The complex result is stored in an output buffer in normal-order. The twiddle factors are contained in separate files that are in bit-reversed order. The core benchmark is given for 1024 samples.	151
FIR Filter (per tap)	Real direct-form FIR filter. It can be used for sample-by-sample filtering. The core benchmark is given per sample.	0.003125
IIR Filter (per biquad)	Each biquad section is implemented using Direct-form II. The core benchmark is given per sample.	0.0125
Viterbi Decoder	Based on 189 point block length, 1/2 rate soft-decision decoder.	96

1. Core clock frequency is 160 MHz, resulting in an instruction cycle time of 6.25 ns.
2. These benchmarks represent the execution time of two algorithms executing simultaneously when both DSP cores are used.

ADSP-21000 SHARC® DSP Family
Real Time, Multiprocessing Leader

The Analog Devices SHARC® DSP family features a "super" Harvard architecture optimized to enable a variety of real-time embedded applications. These 32-bit DSPs allow users to program with equal efficiency in both fixed-point and floating-point arithmetic. The unique memory architecture - two large on-chip, dual-ported SRAM blocks coupled with the sophisticated I/O processor - gives the SHARC DSPs the bandwidth for sustained high-speed computations, just as it should be for real-time embedded DSP development.

Code-compatibility helps to keep development time at a minimum, and maximize our customers' software investments.

The original Single Instruction Single Data (SISD) SHARC DSPs feature a broad range of memory sizes and price points. For very high performance applications, ADI has extended the architecture to a code-compatible, Single Instruction Multiple Data (SIMD) platform.

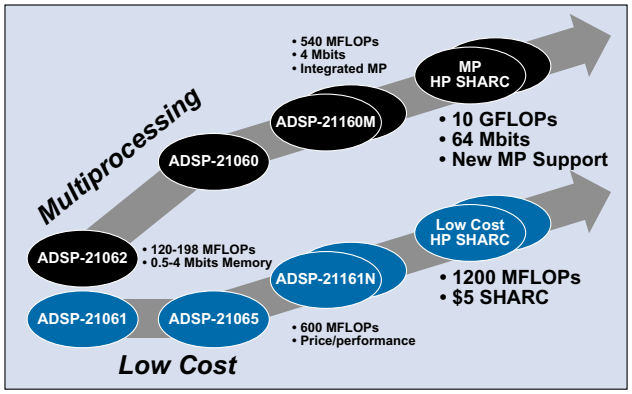
The popularity of SHARC DSPs is evident in our leadership in multiprocessing applications. Patented link port technology has helped establish SHARC as a de facto standard. Future generations of this high-performance solution will continue to deliver the horsepower required for the most demanding multiprocessing applications - those that require clusters of versatile

Applications

- Prosumer Audio
- 3D Graphics
- Arcade Games
- Imaging
- Video Conferencing
- Medical Imaging
- Radar and Sonar Guidance
- Audio Equipment
- Call Processing
- Speech Recognition
- Cellular Basestations
- Instrumentation

SHARC Roadmap

Commitment to Code Compatibility into Tomorrow



32-BIT Generic	Package	Max MIPS	Vcc	On-Chip SRAM	Serial Ports	Price*
ADSP-21160N	B	90	1.9/3.3V	4 Mbits	2	$179.00
ADSP-21160M	B	80	2.5/3.3V	4 Mbits	2	$179.00
ADSP-21161N	B	100	1.8/3.3V	1 Mbit	2	$39.00
ADSP-21065L	S, CA	66	3.3V	544 Kbits	2	$34.50
ADSP-21062/L	B,S	40	3.3/5V	2 Mbits	2	$98.00
ADSP-21061/L	S	50	3.3/5V	1 Mbit	2	$58.00
ADSP-21060/L	B,S	40	3.3/5V	4 Mbits	2	$245.00

Package: B = Plastic Ball Grid Array (PBGA)
G = Ceramic Pin Grid Array (PGA)
S = Plastic Quad Flat Pack (PQFP)
CA = Mini Ball Grid Array (MBGA)
* US Dollars. Lowest grade suggested resale price per unit in 100 unit quantities

ADSP-21160
Single Instruction Multiple Data SHARC

Features

- 540 MFLOPS (32-bit floating-point) peak operation
- 540 MOPS (32-bit fixed-point) peak operation
- 90 MHz core operation, 11 ns cycle time
- 92 µs 1024-point comlex FFT benchmark with bit reversal
- Code compatible with first generation SHARC
- SIMD core includes 2 multipliers, 2 ALUs, 2 shifters, and 2 register files
- 4 Mbits on-chip dual-ported SRAM
- Division of SRAM between program and data memory is selectable
- Core can fetch four 32-bit words from memory in a single processor cycle using two 64-bit wide buses
- Dual data address generators with modulo and bit-reverse addressing
- Efficient program sequencing with zero overhead looping—single-cycle loop setup
- IEEE JTAG standard 1149.1 test access port and on-chip emulation
- 32-bit single-precision IEEE floating-point data type and 40-bit extended precision floating-point data type support
- 32-bit fixed-point formats, integer and fractional, with 80-bit accumulators in both processing elements
- 14 channels of zero-overhead DMA
- Glueless connection for scaleable DSP multiprocessing architectures
- Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-21160s plus host
- Six 100 Mbytes/sec link ports for point-to-point connectivity and array multi-processing
- 2.5 volt core, 3.3 volt I/O (80 MHz 21160M)
- 1.9 volt core, 3.3 volt I/O (90 MHz 21160N)

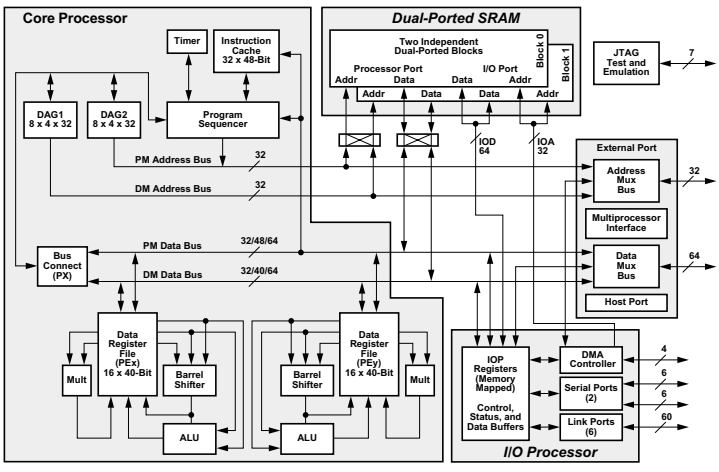
Applications

- Cellular Base Stations
- Call Processing
- Speech Recognition
- Instrumentation
- 3D Graphics Acceleration for Workstations and Arcade Video Games
- Imaging
- High End Audio
- Radar and Sonar

Model	MHZ	Pin/Pkg	Price
ADSP-21160MKB-80	80	400-PBGA	$179.00
ADSP-21160NKB-90	90	400-PBGA	$179.00

M indicates 2.5V operation
N indicates 1.9V operation
K = Commercial Temp (0ºC to 85ºC)

Development Tools	
ADDS-2116X-WKSHP	DSP Workshop
ADDS-21160M-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	Complete Software Pkg
ADDS-MTN-ICE	ISA-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator
ADDS-APEX-ICE	USB-Based Emulator
ADDS-TREK-ICE	Ethernet-Based Emulator



SHARC

http://www.analog.com/dsp

ANALOG DEVICES

ADSP-21160 vs. TMS320C6x Comparison

Features	TMS320C62x	TMS320C67x	ADSP-21160 SHARC
IEEE 32-bit floating-point-support	No	Yes	Yes
Native 32-bit fixed-point-support	No	No	Yes
Dual-ported internal memory	No	No	Yes
Built-in multiprocessing support	No	No	Cluster and link
Number of DMA channels	4	4	14
Zero overhead DMA support[1]	No	No	Yes
Number of registers	32	32	128
Accumulator size	40 bits	40 bits	80 bits
64-bit product support	No	Yes	Yes
Memory bandwidth[2]	64 bits/cycle	128 bits/cycle	128 bits/cycle
Software loop support	No interrupts for compact loops	No interrupts for compact loops	Interrupts allowed in compact loops
Assembly complexity[3]	Highly complex	Highly complex	Algerbraic assembly language
Number of circular buffers supported[4]	8	8	32
Conditional execution support	Requires extra register	Requires extra register	Dedicated conditional logic
FIR filter code size[5]	100 instructions	100 instructions	25 instructions
Package size	35mm, 352 ball	35mm, 352 ball	27mm, 400 ball

1 The TMS320C6x does DMA by stealing cycles from the core.
2 “Memory bandwidth” refers to the data path widths between the register file and memory.
3 Hand-optimized TMS320C6x assembly language must be written in a highly-complex, non-single assignment form.
4 The TMS320C6x only allows two different lengths of circular buffers and the lengths must be power of two.
5 TMS32062xx Programmer’s Guide page 4-112.

ADSP-21161N

Low-Cost Single Instruction Multiple Data (SIMD) SHARC

The ADSP-21161N is the newest member of the high performing SIMD SHARC DSP family. This device offers the industry's highest 32-bit DSP performance at a price that will support consumer applications.

Features

- 3.3 Volt external / 1.8 Volt Internal
- 1 Mbit on chip SRAM
- 14 Zero-Overhead DMA Channels
- SPI-compatible port for serial host and peripheral control
- 4 SPORTs supporting 128 Channel TDM and I^2S
- 12 General Purpose I/O lines, 4 IRQ lines, 1 Timer
- Code-compatible to all other SHARC Family DSPs
- Single-Instruction-Multiple-Data (SIMD) computational architecture – two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file
- 100 MHz (10 ns) core instruction rate 600 MFLOPS peak and 400 MFLOPs sustained performance
- Dual Data Address Generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- IEEE 1149.1 JTAG standard test access port and on-chip emulation
- 225-ball 17x17 mm PBGA package

Model	MHZ	Pin/Pkg	Price* (100-499)
ADSP-21161NKB-100x	100	225-PBGA	$39.00

X indicates pre-release silicon
N indicates 1.8 volt operation
* Budgetary pricing – subject to change

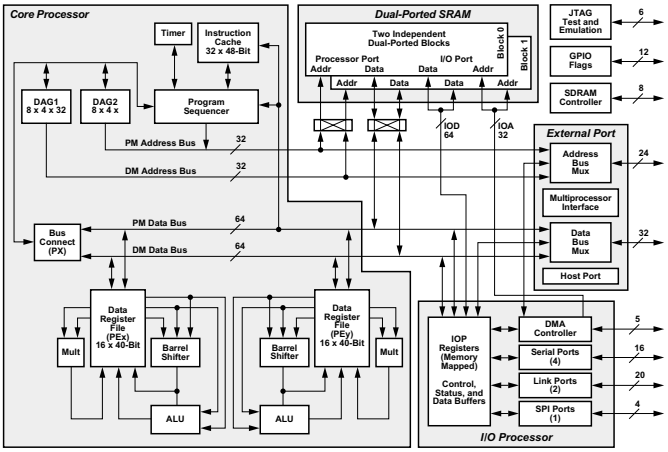
Development Tools	
ADDS-2116X-WKSHP	DSP Workshop
ADDS-21161N-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	Complete Software Pkg
ADDS-MTN-ICE	ISA-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator
ADDS-APEX-ICE	USB-Based Emulator
ADDS-TREK-ICE	Ethernet-Based Emulator

Benefits

- Two 100 Mbyte/S link ports simplify connection and communication in multiprocessing systems
- 14 zero overhead DMA channels mean no cycles stolen from the core to move data on and off chip
- Cluster multiprocessing enables universally addressable memory system
- SDRAM controller for controlling large banks of DRAM
- 4 serial ports allow for 16 channels of data to be transferred in/out of the DSP

Applications

- Video Phones
- Power Line Modems
- Finger Print Recognition
- Medical Equipment
- Multi Access Motor Control
- Automatic Car Systems
- Professional Audio
- Voice Recognition
- MP3 Encoder
- ADSL/Cable Test Equipment
- Global Positioning
- Telephony
- High End Consumer Audio
- Digital Broadcast Radio



http://www.analog.com/dsp

ANALOG DEVICES

ADSP-21065L

Low-Cost Entry-Point to the SHARC DSP Family

Features

- 16K 32-bit dual-ported on-chip memory (544 KBits configurable)
- 64M x 32-bit word external address space
- 198 MFLOPS (32-bit floating-point)
- 198 MOPS (32-bit fixed-point)
- Glueless SDRAM interface
- 2 serial transmit/receive ports support 32-channel TDM
- I²S mode supports up to 16 channels
- 2 timers with event capture and PWM options
- 12 programmable I/O pins
- 10 DMA channels
- Glueless multiprocessing with 2 ADSP-21065Ls
- Code compatible with all SHARC family members
- 3.3 volt, 208-pin MQFP, 196 MBGA

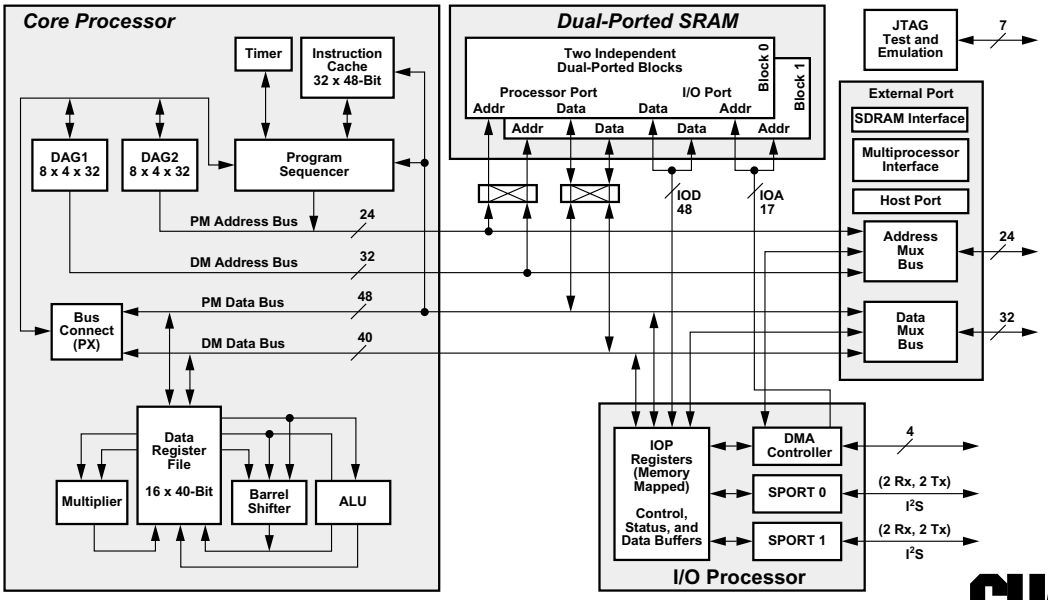
Applications

- Digital Audio
- Keyless Entry Using Voice Analysis/recognition
- Bar Code Scanners
- Imaging
- Ultrasound Epuipment
- Digital Oscilloscopes
- Fingerprint Recognition

Model	MHz	Pin/Pkg	Price (100-499)
ADSP-21065LKS-240*	60	208-MQFP	$34.50
ADSP-21065LKS-264	66	208-MQFP	$43.00
ADSP-21065LKCA-240	60	196-MBGA	$42.50
ADSP-21065LKCA-264	66	196-MBGA	$44.20
ADSP-21065LCS-240	60	208-MQFP	$43.00

C = Industrial (-40ºC to +100ºC)
K = Commercial (0ºC to +85ºC)
* L Indicates 3.3 Volt Operation

Development Tools	
ADDS-2106X-WKSHP	DSP Workshop
ADDS-21065L-EZLITE	Evaluation Kit
VDSP-SHARC-PC-FULL	Complete Software Pkg
ADDS-MTN-ICE	ISA-Based Emulator
ADDS-SUMMIT-ICE	PCI-Based Emulator
ADDS-APEX-ICE	USB-Based Emulator
ADDS-TREK-ICE	Ethernet-Based Emulator



ADMC Motor Control Family
Embedded DSP-Based Motor Controllers

The ADMC family of embedded DSP-based Motor Controllers integrate 16-bit, fixed point DSPs with software and analog circuitry optimized for motor control applications. All processors are fully code compatible, allowing for additional features and enhanced performance, while protecting the software development investment.

Development Tools

Generic specific evaluation and development tools are available for each ADMCxxx device. Development tool kits include everything required to quickly and easily develop user specific applications including:

- VisualDSP-based motion control debugger
- Connector board
- Compiler, linker, assembler
- Serial cable
- Example software
- User documentation and reference guides
- Modular processor board

Motor Control applications support can be obtained at mcapps@analog.com. Users can also obtain additional support, free software upgrades, and sample code by visiting the Motor Control Web site at www.analog.com/motorcontrol/

Embedded DSP Motor Control Selector Guide

		Memory						
Device	MIPS	Program RAM	Program FLASH	Program ROM	Data RAM	ADC	Motor Control Peripherals	Package Options
ADMC401	26	2K x 24-bits		2K x 24-bits	1k x 16-bits	8 Channel 12-bit Simultaneous Sampling	• 3 Phase 16-bit PWM • Aux PWM • Encoder Interface • 12 PIOs • 2 Serial Ports • Power-On-Reset	144 Pin LQFP
DashDSP™ • ADMCF326 • ADMC326 • ADMCF327 • ADMC327 • ADMCF328 • ADMC326	20	512 x 24-bits	4K x 24-bits (F32x)	4K x 24-bits (32)	2k x 16-bits	• 6 Channel 10-bit (F326/326) (F327/327) • 5 Channel 10-bit + Isense (F328/328)	• 3 Phase 16-bit PWM • PWM SR Mode (F327/327) • Aux PWM • 9 PIOs • Power-On-Reset	28 Pin SOIC or PDIP
ADMC331	26	2K x 24-bits		2K x 24-bits	1k x 16-bits	• 7 Channel 10-bit	• 3 Phase 16-bit PWM • Aux PWM • 24 PIOs	80 Pin TQFP
ADMC300	25	4K x 24-bits		2K x 24-bits	1k x 16-bits	• 5 Channel 16-bit Sigma Delta (76 dB SNR Typical Converters)	• 3 Phase 16-bit PWM • Aux PWM • Encoder Interface • 12 PIOs • 2 Serial Ports	80 Pin TQFP

ADMCF32x/ADMC32x

28-Pin DSP-Based Motor Controllers with Flash Memory

Features

- Integrated ADC subsystem
  - ADMCF328/ADMC328 - Five 10-bit analog inputs plus one dedicated analog current sense (5X amplifier plus PWM trip)
  - ADMCF326/7/ADMC326/7 Six 10-bit analog inputs
  - Internal voltage reference
- Three phase 16-bit PWM generation unit
  - Switched reluctance specific PWM generation unit (ADMCF327/ADMC327 only)
- Two 8-bit auxiliary PWM outputs
- 20 MIPS fixed point DSP core
  - 4K x 24-bit program flash memory (ADMCF32x only)
    - Three independently written sectors
    - Non-volatile security lock bits
    - 10K erase/program cycles
  - 4K x 24-bit program memory ROM (ADMC32x only)
  - 512 x 24-bit program memory RAM
  - 512 x 16-bit data memory RAM
- 9 Bits of programmable digital I/O
- Integrated power-on-reset function
- Pin for pin compatible ROM options
- 28 pin SOIC or PDIP package options

Model	Temp Range	Instr Rate	Pin PKG	Price (100-499)
ADMCF326BN	Industrial (-40°C	20 MHz	28 Pin PDIP	$15.95
ADMCF326BR	Industrial (-40°C	20 MHz	28 Pin SOIC	$15.95
ADMCF327BN	Industrial (-40°C	20 MHz	28 Pin PDIP	$15.95
ADMCF327BR	Industrial (-40°C	20 MHz	28 Pin SOIC	$15.95
ADMCF328BN	Industrial (-40°C	20 MHz	28 Pin PDIP	$15.95
ADMCF328BR	Industrial (-40°C	20 MHz	28 Pin SOIC	$15.95
A unique model number is assigned to each ROM order received	Industrial (-40°C to 85°C) Automotive (-40°C to 85°C)	20 MHz	28 Pin PDIP 28 Pin SOIC	$15.95

Development Tools		
ADMCF326-EVALKIT	ADMCF326 evaluation board and motor control development tools (assembler, linker, debugger)	$395.00
ADMCF327-EVALKIT	ADMCF327 evaluation board and motor control development tools (assembler, linker, debugger)	$395.00
ADMCF328-EVALKIT	ADMCF328 evaluation board and motor control development tools (assembler, linker, debugger)	$395.00

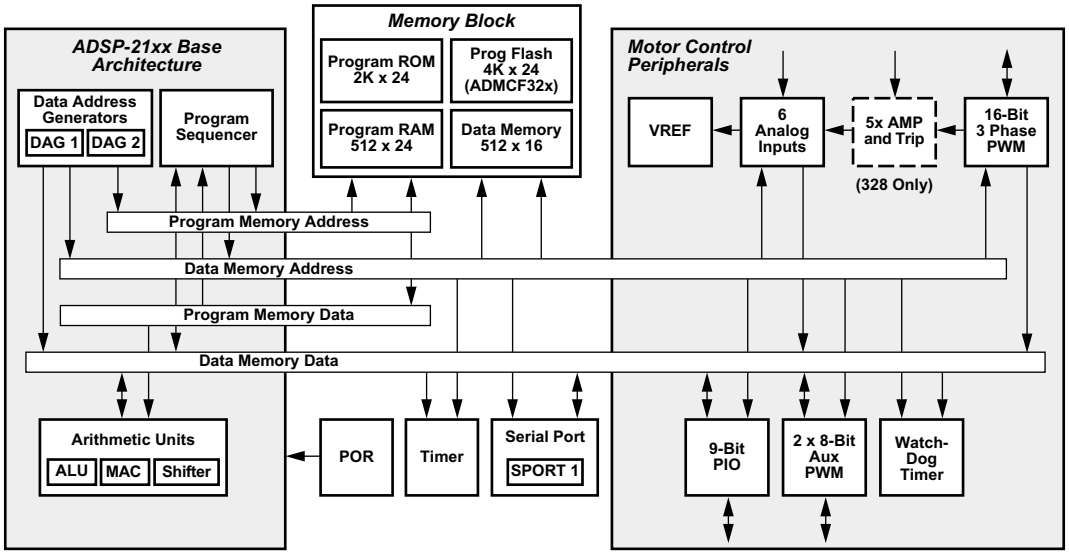
ADMCF32x/ADMC32x

Benefits

- ADC subsystems and peripherals tailored for specific motor types to simplify development
- 28 pin standard package options simplify system design
- 3 Sector on-chip Flash memory allows for in-circuit programming for software upgrade ability and rapid code development
- Integrated Power-On-Reset and precision voltage reference reduce system costs
- Pin for pin compatible ROM device provide low cost high volume option
- Fully Code Compatible with all ADSP-21xx and ADMCxx family products
- Algebraic assembly language for easy programming
- Industrial and Automotive temperature grades

Applications

- Motor types - AC Induction Motors (ACIM), Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM), Switched Reluctance Motors (SRM)
- Industrial variable speed and servo drives
- Uninterruptable power supplies
- Electric vehicles
- Smart sensors/data acquisition systems



http://www.analog.com/motorcontrol

ANALOG DEVICES

ADMC401

Single-Chip, High Performance DSP-Based Motor Controller

Features

- High resolution integrated 12-bit multi-channel ADC (> 70 dB SNR)
  - 8 channel simultaneous sampling (8 channels converted in < 2µ sec)
  - Integrated precision voltage reference
- Three phase 16-bit PWM generation unit
- Two 8-bit auxiliary PWM outputs
- 26 MIPS fixed point DSP core
  - 2K x 24-bit program memory RAM
  - 2K x 24-bit program memory ROM
  - 1K x 16-bit data memory RAM
  - 14-bit adress bus and 24-bit data bus for external memory expansion
- Incremental encoder interface
- Programmable digital I/O
- Integrated power-on-reset

Benefits

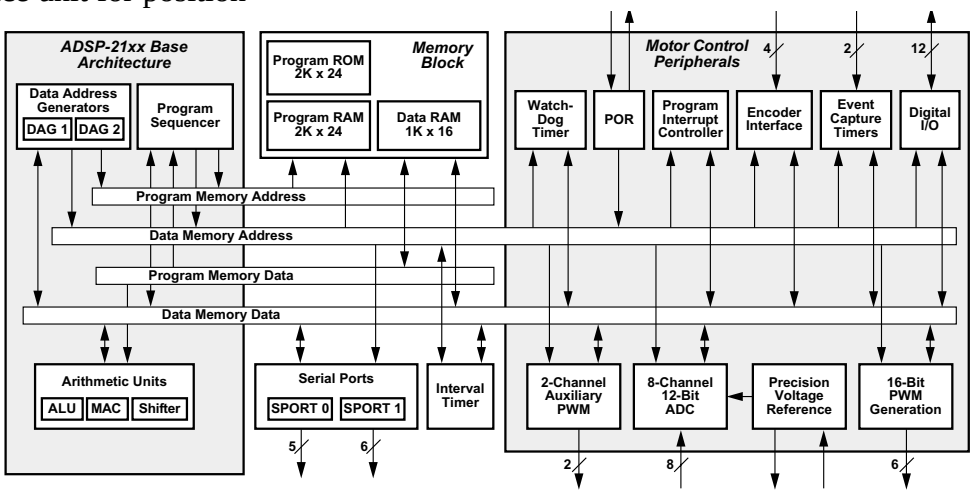
- High performance DSP integrated with fast 12-bit ADC provides for true single chip solution
- Fully code compatible with all ADSP-21xx and ADMCxx family products
- Algebraic assembly language for easy programming
- External address and data bus allows external memory to be added as needed
- Flexible encoder interface unit for position feedback
- Integrated power-on-reset function and voltage reference remove system cost

Applications

- Motor types - AC Induction Motors (ACIM), Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM), Switched Reluctance Motors (SRM)
- Industrial variable speed and servo drives
- Uninterruptable power supplies
- Numerical control machines
- Robotics

Model	Temp Range	Instr Rate	Pin PKG	Price (100-499)
ADMC401BST	Industrial (-40°C to 85°C)	26 MHz	144 Pin LQFP	$24.95

Development Tools	Price
ADMC401-ADEVALKIT ADMC401 evaluation board and motor control development tools (assembler, linker, debugger)	$395.00



ADMC331
Single Chip, DSP-Based Motor Controller

Features

- Seven channel, 10-bit analog-to-digital converter
- Three Phase 16-bit PWM generation unit
- Two 8-bit auxiliary PWM outputs
- 26 MIPS fixed point DSP core
  - 2K x 24-bit program memory RAM
  - 2K x 24-bit program memory ROM
  - 1K x 16-bit data memory RAM
- 24 Bits of programmable digital I/O
- Preprogrammed mathematical functions
- Preprogrammed motor control functions (Vector Transformations)
- 16-bit watchdog timer
- Two double buffered synchronous serial ports

Benefits

- Single chip solution with integrated motor control peripherals simplifies hardware development and reduces system cost
- Preprogrammed mathematical and motor control functions simplify code development
- Auxiliary PWM outputs enable power factor correction for energy efficient motor systems
- Fully code compatible with all ADSP-21xx and ADMCxx family products
- Algebraic assembly language for easy programming

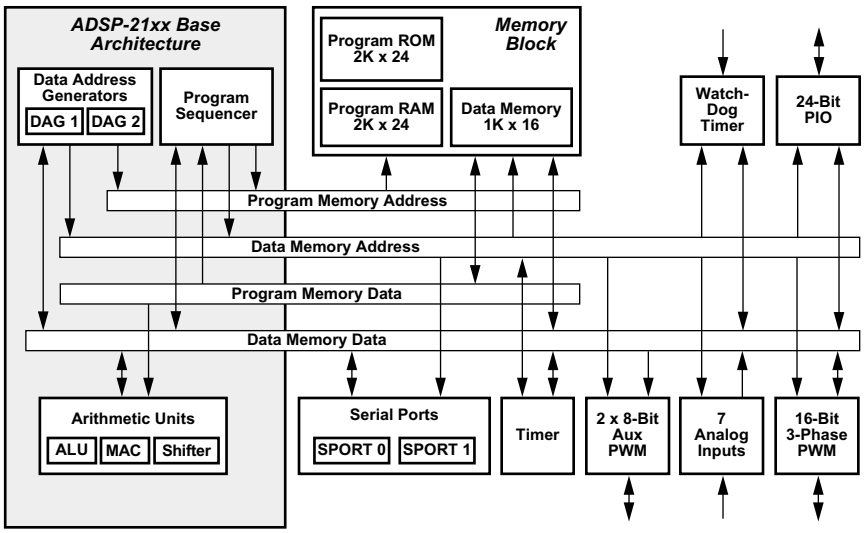
Applications

- Motor Types - AC Induction Motors (ACIM), Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM), Switched Reluctance Motors (SRM)
- Consumer Applications – washing machines, HVAC, refrigerator compressors
- Industrial variable speed drives, pumps electric vehicles

Model	Temp Range	Instr Rate	Pin PKG	Price (100-499)
ADMC331BST	Industrial (-40°C to 85°C)	26 MHz	80 Pin LQFP	$14.95

Development Tools	Price
ADMC331-ADEVALKIT ADMC331 evaluation board and motor control development tools (assembler, linker, debugger)	$395.00

Note: The ADMC331 is recommended for future designs based on the obsoleted ADMC330



http://www.analog.com/motorcontrol

ANALOG DEVICES

ADMC300
High Performance DSP-Based Motor Controller

Features

- High Resolution 16-bit sigma delta analog input system (76 dB SNR)
  - – Five independent ADC channels
  - – Internal voltage reference
- Three phase 16-bit PWM generation unit
- Two 8-bit auxiliary PWM outputs
- 25 MIPS fixed point DSP core
  - – 4K x 24-bit program memory RAM
  - – 2K x 24-bit program memory ROM
  - – 1K x 16-bit data memory RAM
- Incremental encoder interface
- Programmable digital I/O

Benefits

- High performance DSP integrated with high resolution 12-bit ADC provides true single chip solution
- Flexible encoder interface unit for position feedback
- Fully code compatible with all ADSP-21xx and ADMCxx family products
- Algebraic assembly language for easy programming

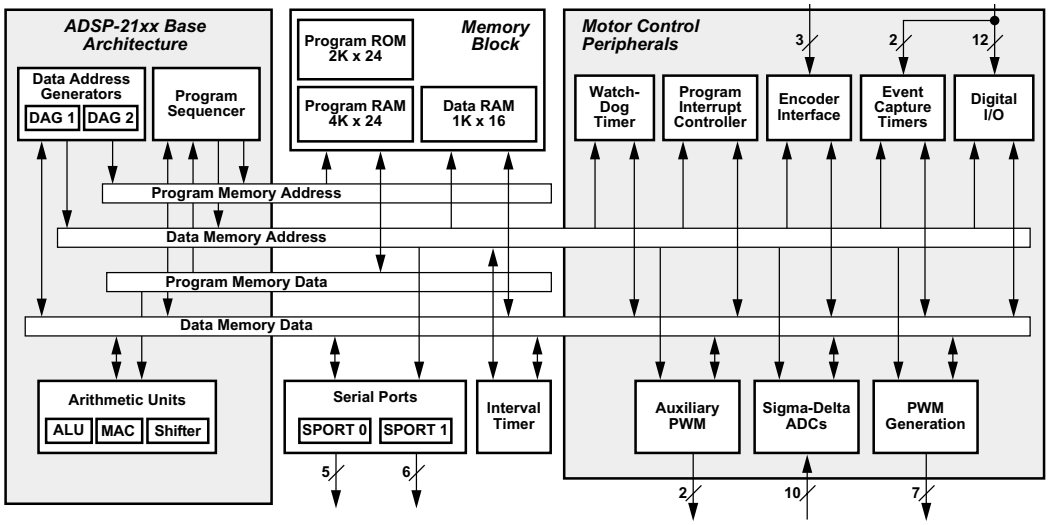
Applications

- Motor types - AC Induction Motors (ACIM), Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM),
- Industrial variable speed and servo drives
- Uninterruptable power supplies
- Electric vehicles
- Smart sensors/data acquisition systems

Model	Temp Range	Instr Rate	Pin PKG	Price (100-499)
ADMC300BST	Industrial (-40°C to 85°C)	25 MHz	80 Pin LQFP	$19.95

Development Tools	Price
ADMC300-ADEVALKIT ADMC300 evaluation board and motor control development tools (assembler, linker, debugger)	$395.00

http://www.analog.com/motorcontrol



Quad-SHARCs AD14060/AD14160

480-MFLOP, Single Package Multiprocessor

The **AD14060** Quad-SHARC is a first generation (CQFP) DSP multiprocessor. Using high-density packaging techniques, the module fits four SHARCs in approximately 30% of the space required using discrete packages.

The **AD14160** Quad-SHARC Ceramic Ball Grid Array (CBGA) puts the power of the first generation AD14060 (CQFP) DSP multiprocessor into a very high density ball grid array package, the module fits four SHARCs in approximately 30% of the space required using discrete packages; now with additional link and serial I/O pinned out, beyond that from the CQFP package.

The core of the multiprocessors is the ADSP-21060 DSP Microcomputer. The AD14X60 modules have the highest performance-density and lowest cost-performance ratios of any multiprocessors in their class. They are ideal for applications requiring higher levels of performance and/or functionality per unit area.

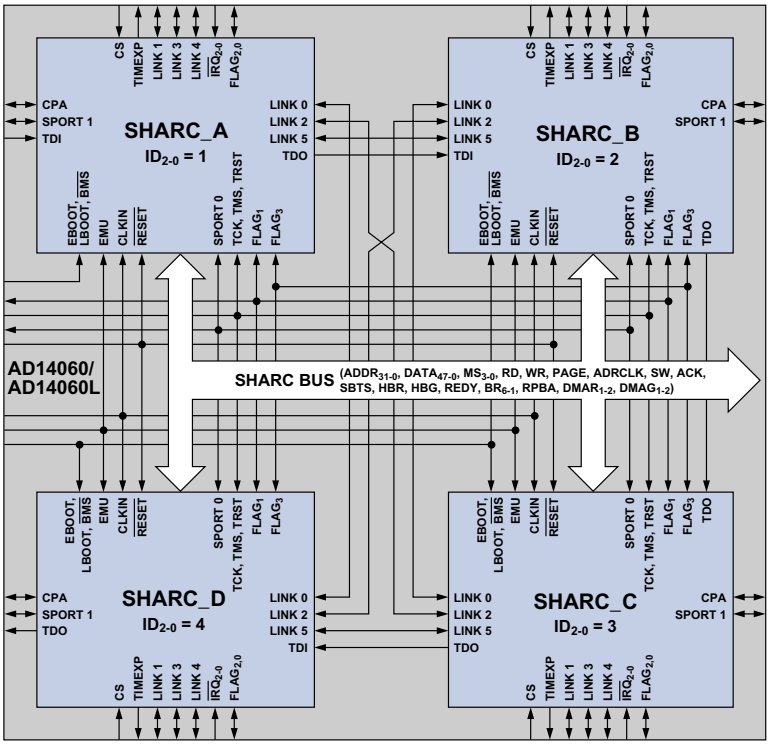
The AD14060/AD14160 take advantage of the built-in multiprocessing features of the ADSP-21060, to achieve 480 peak MFLOPS with a single chip type, in a single package. The on-chip SRAM of the DSPs provides 16 Mbits of on-module shared SRAM. The complete shared bus (48-bit data, 32-address) is also brought off-module for interfacing with expansion memory and/or other peripherals.

Applications

Multi-SHARC designs with tight area/volume constraints, such as large array and image processors, smart missiles, avionics, and others will benefit. The AD14060/AD14160 are available as both industrial and MIL-SMD grade parts in 5V (AD14060/AD14160) or 3.3V (AD14060L/AD14160L) versions.

Competition

With 480 MFLOPS of throughput, the AD14060/AD14160 have no close competitors. TI's Dual C40 MCM provides a similar function, but delivers only 80 MFLOPS in a significantly larger package, and roughly equivalent cost. The Quad-SHARC AD14060/AD14160 is targeted to be priced such that users can take advantage of system cost advantages of using MCMs.



AD14060 Functional Block Diagram

http://www.analog.com/milsystems

ANALOG DEVICES

Quad-SHARCs AD14060/AD14160

Development Tools

The AD14060-AD14160 is supported with a complete set of software and hardware development tools, including an EZ-LAB® in-circuit emulator, and development software.

Features

- ADSP-21060 core processor (. . . x4)
- 480 MFLOPS Peak, 320 MFLOPS sustained
- 25 ns instruction rate, single-cycle instruction execution - each of 4 processors
- 16 Mbit shared SRAM (internal to SHARC's)
- 4 gigawords addressable off - module memory
- 48-bit shared memory bus, 48-bit data bus
- Full 32-bit address bus
- Interrupts, flag pins, and timers are also avail able as I/O
- 32-Bit single precision and 40-Bit extended precision IEEE floating point data formats, or 32-Bit fixed point data format
- User configurable boot modes, bus priority, and other features with control lines
- IEEE JTAG standard 1149.1 test access port and on-chip emulation

AD14060

– Twelve 40 Mbyte/s link ports (3per SHARC) accessible to/from the outside world
– Four link ports connected internally in a ring configuration
– Four 40 Mbit/s independent serial ports (one from each SHARC)
– One 40 Mbit/s common serial port
– Ceramic quad flat pack with enhanced I/O
– Low-profile 2.05" 308 lead ceramic quad flat pack package

AD14160

– Sixteen 40 Mbyte/s link ports (per SHARC) accessible to/from the outside world
– Eight link ports connected internally in ring configuration
– Eight 40 Mbit/s independent serial ports (two from each SHARC) available from outside
– Ceramic ball grid array QUAD-SHARC with enhanced I/O
– Low-profile 1.85" ceramic ball grid array package

For any further inquiries, please contact MCP Marketing in Greensboro, NC @ 336-668-9511

http://www.analog.com/milsystems

dspConverter™
Integrated DSP and Data Converter for Voice Processing

ADI's dspConverters feature our industry leading data converters, 16-bit fixed-point DSPs and flash memory all packed into one small (14 mm x 22 mm) BGA package.

The analog front ends are based on our AD733xx family which include 16-bit linear codecs, input/output conditioning circuitry and a flexible serial interface. The DSPs are based on the ADSP-218x family.

Analog Front Ends (AFEs)

The analog front ends are much more than codecs. Each channel includes:

- Sigma-delta DAC
- Sigma-delta ADC
- PGA for each encoder and decoder
- Input conditioning circuitry
- Reference
- SPORT

No Digital Feedthrough Problems

One of the critical aspects of mixed-signal design is digital feedthrough from high-speed processors to high-resolution analog circuitry. This is fully addressed in our dspConverters with careful circuit layout and synchronization of clocks. Test results have verified that clock noise is absent from the digitized analog spectrum even when the DSP is running at full speed.

Converter Performance and Group Delay

The converters are fully specified with SNR+THD figures of 78 dB for the encoders and 77 dB for the decoders. A notable feature of the performance specification is it's clarity.

Group delay can be critical in noise cancellation applications. It's important to cancel the noise as close to the source as possible. Delays increase modeling errors, require larger filters and inhibit random noise cancellation systems. All analog front ends in the family offer group delays, which are 25 µs for the encoder and 50 µs for the decoder.

dspConverter Selection Table

Generic	AFE Channels	DSP	Program Memory	Data Memory	Price*
AD73411-40	1	52 MIPS	8K	8K	$17.64
AD73411-80	1	52 MIPS	16K	16K	$21.17
AD73422-40	2	52 MIPS	8K	8K	$20.41
AD73422-80	2	52 MIPS	16K	16K	$23.47
AD73460-80	6-Ch ADC	52 MIPS	16K	16K	$23.47

* US Dollars. Lowest grade suggested resale price per unit in 100 unit quantities

http://www.analog.com/dspconverter

AD73411
Low Power Analog Front End with DSP

Features

AFE PERFORMANCE
- 16-Bit A/D converter
- 16-Bit D/A converter
- Programmable input/output sample rates
- 76 dB ADC SNR
- 77 dB DAC SNR
- 64 kS/s maximum sample rate
- –90 dB crosstalk
- Low group delay (25 µs typ per ADC channel, 50 µs typ per DAC channel)
- Programmable input/output gain
- On-chip reference

DSP PERFORMANCE
- 19 ns instruction cycle time @ 3.3 Volts, 52 MIPS performance
- Single-cycle instruction execution
- Single-cycle context switch
- 3-Bus architecture allows dual operand fetches in every instruction cycle
- Multifunction instructions
- Power-down mode featuring low CMOS standby
- Power dissipation with 400 cycle recovery from power-down condition
- Low power dissipation in idle mode

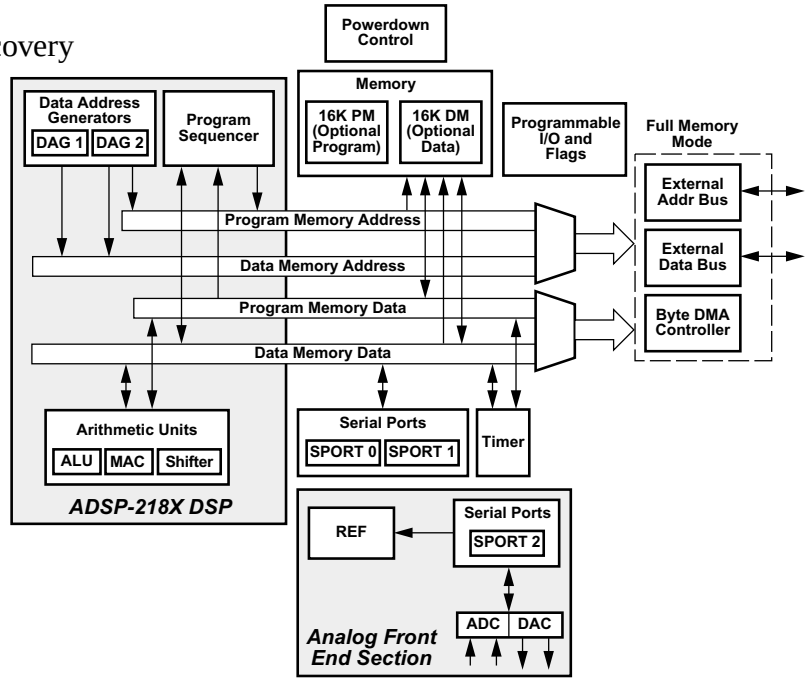
Benefits

- Extensive analog front ends include A/Ds, D/A, PGAs, reference and input conditioning circuitry
- Reduced design risk – all the interface design work is done
- Programmable, high-speed DSP based on ADSP-218x Family

Applications

- General Purpose Analog I/O
- Speech Processing
- Cordless and Personal Communications
- Telephony
- Wireless Local Loop
- Active Control of Sound and Vibration
- Data Communications

Model	AFE CHNS	Prog Data Memory	Pin PKG
AD73411-40	1	8/8K	119 PBGA
AD73411-80	1	16/16K	119 PBGA



AD73422
Dual Low Power Analog Front End with DSP

Features

AFE PERFORMANCE
- 16-Bit A/D converter
- 16-Bit D/A converter
- Programmable input/output sample rates
- 76 dB ADC SNR
- 77 dB DAC SNR
- 64 kS/s maximum sample rate
- –90 dB crosstalk
- Low group delay (25 µs typ per ADC channel, 50 µs typ per DAC channel)
- Programmable input/output gain
- On-chip reference

DSP PERFORMANCE
- 19 ns instruction cycle time @ 3.3 Volts, 52 MIPS performance
- Single-cycle instruction execution
- Single-cycle context switch
- 3-Bus architecture allows dual operand fetches in every instruction cycle
- Multifunction instructions
- Power-down mode featuring low CMOS standby
- Power dissipation with 400 cycle recovery from power-down condition
- Low power dissipation in idle mode

http://www.analog.com/dspconverter

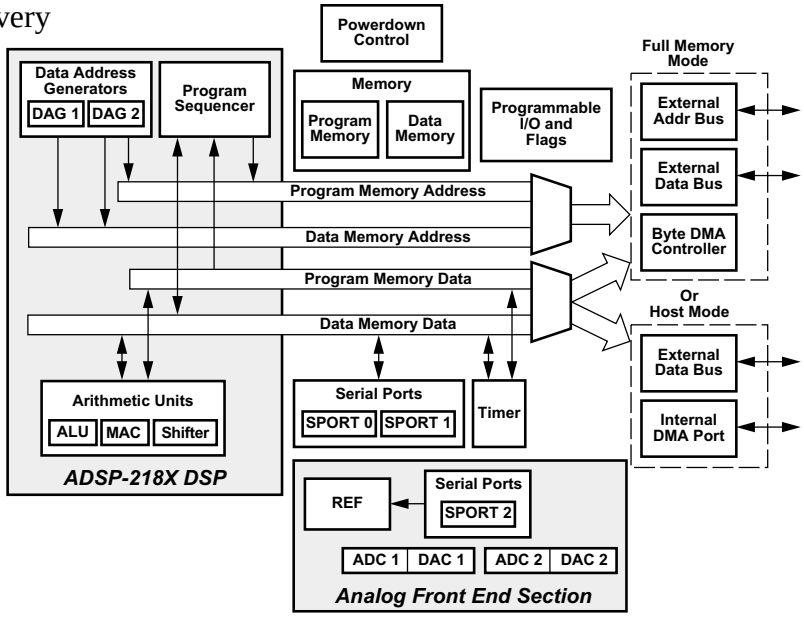
Benefits

- Extensive analog front ends include A/Ds, D/A, PGAs, reference and input conditioning circuitry
- Reduced design risk – all the interface design work is done
- Programmable, high-speed DSP based on ADSP-218x Family

Applications

- General Purpose Analog I/O
- Speech Processing
- Cordless and Personal Communications
- Telephony
- Wireless Local Loop
- Active Control of Sound and Vibration
- Data Communications

Model	AFE CHNS	Prog Data Memory	Pin PKG
AD73422-40	2	8/8K	119 PBGA
AD73422-80	2	16/16K	119 PBGA



http://www.analog.com/dspconverter

Software and Systems Technologies (SST)

Marketplace pressures of the newest technologies, faster time to market, and ever-lower systems costs drive leading OEMs to look for the newest, fastest ways to introduce their products to their customers.

To meet this need, Analog Devices Inc. offers numerous chipset and algorithm solutions with reference designs and third party support in emerging and high growth market segments such as:

- Audio Solutions
- Video Communications Solutions
- Energy Meter Solutions
- Communications & Telephony Solutions
- Global Positioning Solutions
- Embedded Modems
- Standalone Embedded Modems
- Internet Modems
- Wireless Local Loop

ADSST-MPEG-EVAL01
Single-Chip MP3 Encoder/Decoder

Features

- Decodes MPEG1 Audio Layer 3 (MP3)
- Encodes MPEG1 Audio Layer 3 (MP3)
- Fully complies with the ISO/IEC 11172-3 audio standard
- Supports half-sampling frequencies of 16, 22.05 and 24 kHz and full sampling frequencies of 32, 44.1 and 48 kHz per channel
- Supports 8 kbps to 160 kbps bit rates for half-sampling frequencies, 32 kbps to 320 kbps for full sampling frequencies
- Compact single-chip chipset or 85 mm x 60 mm x 30 mm board

Benefits

- Operates in real time and processes all combinations of the algorithms
- Directly encodes MP3 onto the device flash memory
- Requires no external SRAM or SDRAM
- Includes bass boost and equalizer

Applications

- Digital Audio
- Portable, Handheld, and Automotive Audio
- CD-Ripping
- Home Theatre
- Internet Audio
- Internet Distribution of Original Music
- Previewing Favorite Artists

Model	MHz	Pin/Pkg
ADSST-MPEG-EVAL01	75	Reference Design

ADSST-DAP-EVAL01
Single-Chip MP3 Encoder/Decoder

Features

- Decodes MPEG1 Audio Layer 3
- Encodes MPEG1 Audio Layer 3
- Fully complies with the ISO/IEC 11172-3 audio standard
- Supports half-sampling frequencies of 16, 22.05 and 24 kHz and full sampling frequencies of 32, 44.1 and 48 kHz per channel
- Supports 8 kbps to 160 kbps bit rates for half-sampling frequencies, 32 kbps to 320 kbps for full sampling frequencies
- Compact single-chip chipset or 85 mm x 60 mm x 30 mm board

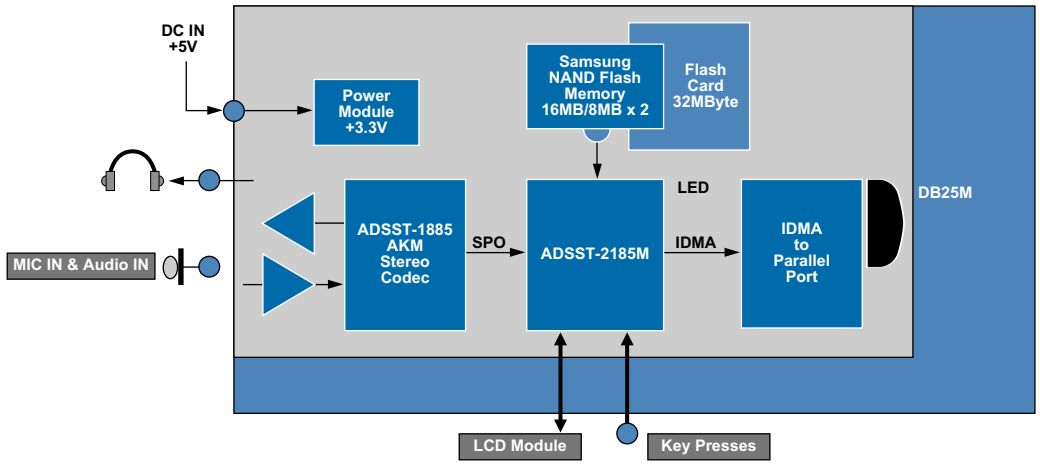
Applications

- Digital Audio
- Portable, Handheld, and Automotive Audio
- CD-Ripping
- Home Theatre
- Internet Audio
- Internet Distribution of Original Music
- Previewing Favorite Artists

Model	MHz	Pin/Pkg
ADSST-DAP-EVAL01	75	Reference Design

Benefits

- Supports multiple storage types
- Operates in real time
- Directly encodes MP3 onto the device
- Requires no external SRAM or SDRAM
- Supports watermarking technology and DRM
- Includes bass boost and equalize



DAP 1.0 Block Diagram (Recorder)

http://www.analog.com/solutions

ANALOG DEVICES

ADSST-PEGASUS-SDK

Melody Floating-Point Audio Encoders/Decoders

Features

- Decodes DTS Discrete 6.1, DTS-ES Matrix 6.1, DTS Neo:6, Dolby Digital, Dolby Pro Logic, Dolby Pro Logic II, Dolby Headphone, HDCD, MPEG1 Audio Layer 3 (MP3), MPEG1 Audio Layers 1 and 2, AAC, PCM, MLP SRS 3D, Wave Surround, Stereo
- Post-Processes THX Surround EX, THX Select, THX Ultra
- Encodes Dolby Digital Consumer Encoding (DDCE) and MPEG1 Audio Layers 1, 2, and 3 (MP3)
- Autodetects and displays bitstream information. Automatically applies appropriate or selected decoder
- Supports sampling frequencies of 16, 22.1, 24, 32, 44.1, 48, 88.2, 96 KHz
- Supports 32 kbps to 4,096 kbps bit rates
- 32-bit floating-point programmable implementation facilitates software upgrades

Benefits

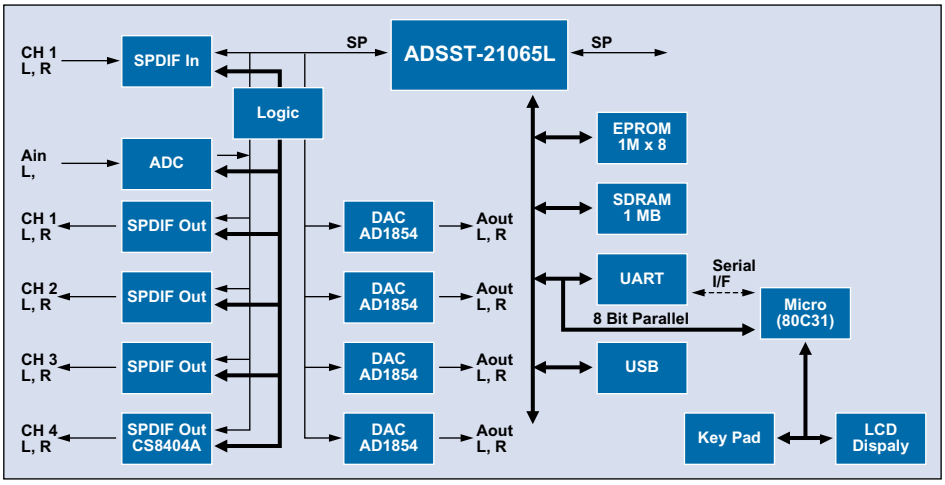
- Decodes latest 6.1-channel algorithms from DTS, Dolby
- Supports multiple audio formats

Applications

- Digital Audio
- Portable, Handheld, and Automotive Audio
- Set-Top Boxes
- Home Theatre
- Internet Audio
- Audio DVDs
- DVD, CD, MLP Players

Model	MHz	Pin/Pkg
ADSST-21065LKST-264	66	PQFP
ADSST-21061L	44	PQFP
ADSST-PEGASUS-SDK	66	Reference Design

http://www.analog.com/solutions



PEGASUS-II Audio Reference

DSP Technical Training Workshops

Description

The DSP System Development and Programming workshops are comprehensive, hands-on workshops. The workshops are geared towards people who have a working knowledge of microprocessors and want to learn how to use Analog Devices DSPs. These courses cover the DSP architecture, assembly language syntax, IO interface, hardware and software development tools, and C compiler. Throughout the workshop, attendees learn how easy it is to use Analog Devices' DSPs from lecture sessions and hands-on exercises.

Locations and Schedules

The workshops are offered monthly in North America. Workshop schedules and more details on DSP workshops are also available on the web site.

How to Register

To enroll, customers should register online at the Analog Devices web site at:
http://www.analog.com/dsp/training
You will be notified when your seat is confirmed.

ADSP-218x Workshop

This is a 3-day workshop which covers the ADSP-218x family of DSPs and development tools. For registration and price, contact Momentum Data Systems via e-mail at sales@mds.com, or by phone at 714-378-5805.

Part Number: ADDS-218x-WKSP Price: Contact Momentum

ADSP-2106x Workshop

This is a 3.5 day workshop which covers all the ADSP-2106x DSPs including the ADSP-21065L and development tools. For registration and price, contact Melinda Rosauro at BBD Electronics at MRosauro@bbd.ca or 905-821-7800 X110.

Part Number: ADDS-2106x-WKSP Price: Contact BBD

ADSP-2116x Workshop

This is a 3.5 day workshop which covers ADSP-21160 and development tools.

Part Number: ADDS-2116x-WKSP Price: $1375.00

ADSP-219x Workshop

This is a 3.5 day workshop which covers the ADSP-219x family of DSPs and development tools.

Part Number: ADDS-219x-WKSP Price: $1375.00

http://www.analog.com/dsp/training

ADI Support for Universities

The ADI DSP University Program provides the next generation of engineers with DSP knowledge to help them compete in the industry of tomorrow.

The ADI DSP University Program offers:

- Complete DSP Software and Hardware Tools to set up a DSP LAB
- Teaching material to help design experiments
- Priority technical support to professors

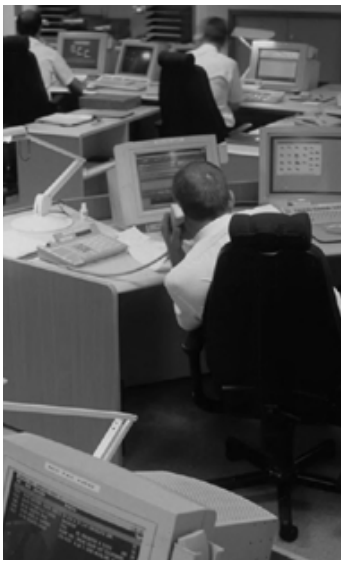
Analog Devices DSP Technology is easy to teach:

- DSP architectures that are the simplest to program in the industry
- Simple instruction sets
- High levels of SRAM integration

Hundreds of universities in 37 countries use ADI DSPs for teaching and research

To request a University donation or learn more, go to:

http://www.analog.com/industry/dsp/university.html



DSP Literature Selection Guide

Title	Where to Order or Download	Publication Number	Price
ADSP-2100 Family Publications			
Scientist and Engineer's Guide to DSP	From Dist. through SAP	SE_Guide_to_DSP	$40.00
DSP Designer's Reference	Lit Center	DSP-Solutions-2001	NC*
ADSP-2100 Family User's Manual	Lit Center	82-000780-03	NC
ADSP-2100 Family 16-Bit Tools Publications			
VisualDSP Debugger Guide & Reference	From Dist. through SAP	VDSP-DUG	$25.00
Debugger Tutorial (for the ADSP-21xx)	www.analog.com/dsp	82-000806-02	NC
ADSP-219x DSP Instruction Set Reference	Lit Center	82-000390-087	NC
ADSP-2100 Family Assembler/Simulator Manual	From Dist. through SAP	ADSP-21XX-DSW-ML	$20.00
ADSP-2100 Family C Tools User Guide	From Dist. through SAP	ADSP-21XX-CTOOL-ML	$25.00
ADSP-2100 Family C-Runtime Library Reference	From Dist. through SAP	ADSP-21XX-EZ-MAN	$10.00
ADSP-2181 EZ-KIT Lite Reference	www.analog.com/dsp	82-000779-01	NC
ADSP-2189M EZ-KIT Lite Evaluation System Manual	www.analog.com/dsp	82-000333-01	NC
ADSP-218x Family EZ-ICE® Hardware Installation Guide	www.analog.com/dsp	82-000332-01	NC
Release Notes (for ADSP-21xx Family of DSPs)	www.analog.com/dsp	83-000853-06	NC
VisualDSP & ADSP-21xx DSP Tools Release 7.0			
Complete Set of ADSP-21xx VDSP Manuals - includes the following:	From Dist. through SAP	VDSP-21XX-MAN-FULL	$100.00
VisualDSP User's Guide for the ADSP-21xx Family DSPs			
Assembler Manual for the ADSP-218x Family DSPs			
Assembler Manual for the ADSP-219x Family DSPs			
C Compiler & Library Manual for the ADSP-218x Family DSPs			
C Compiler & Library Manual for the ADSP-219x Family DSPs			
Linker & Utilities Manual for the ADSP-21xx Family DSPs			
ADSP-2100 Family Data Sheets			
ADSP-21xx Family (REV. B)	Lit Center	C1891b-10-2/96	NC
ADSP-2104/ADSP-2109 (REV. 0)	Lit Center	C2145-16-7/96	NC
ADSP-2171/2172/2173 (REV. A)	Lit Center	C1984A-6-11/95	NC
ADSP-216x (REV. 0)	Lit Center	C3511-3-10/99	NC
ADSP-2181 (REV. D)	Lit Center	C2041c-3-3/98	NC
ADSP-2183 (REV. C)	Lit Center	C3025c-2.5-2/00	NC
ADSP-2184 (REV. 0)	Lit Center	C3418-2-5/99	NC
ADSP-2184L (REV. 0)	Lit Center	C3419-2-5/99	NC
ADSP-2185 (REV. 0)	Lit Center	C2993-10-3/97	NC
ADSP-2185L (REV. A)	Lit Center	C3189a-3-10/98	NC
ADSP-2185M (REV. 0)	Lit Center	C02047-3.5-10/00	NC
ADSP-2186 (REV. A)	Lit Center	C2999a-2-12/99	NC
ADSP-2186L (REV. A)	Lit Center	C00191a-2.5-8/00	NC
ADSP-2186M (REV. 0)	Lit Center	C02048-3.5-10/00	NC
ADSP-2187L (REV. 0)	Lit Center	C3174-3-7/98	NC
ADSP-2188M (REV. 0)	Lit Center	C01629-2.5-9/00	NC
ADSP-2189M (REV. A)	Lit Center	C3605a-2-3/00	NC
ADSP-2188N (REV. Pr A)	Lit Center	Preliminary	NC
ADSP-2192 (REV. Pr A)	Lit Center	Preliminary	NC

* NC = No charge

** Data Sheets and Manuals Can Also Be Downloaded From the ADI DSP Website

DSP Literature Selection Guide

Title	Where to Order or Download	Publication Number	Price
ADSP-21000 SHARC Family Publications			
ADSP-2106x SHARC Family User's Manual 2nd Edition	Lit Center	E2003a-16-5/97	NC
ADSP-21065L User's Manual & Technical Reference	Lit Center	82-001833-01	NC
ADSP-21160 SHARC Hardware Reference	Lit Center	82-001966-01	NC
ADSP-21160 SHARC Instruction Set Reference	Lit Center	82-001967-01	NC
ADSP-21000 Family Applications Handbook	Lit Center	82-000757-01	NC
A Guide To Multiprocessing Solutions from the DSP Collaborative	Lit Center	G3632-10-7/00 (Rev. A)	NC
ADSP-21000 Family Assembler/Simulator Manual	From Dist. through SAP	ADSP-21XX-DSW-MAN	$20.00
ADSP-21000 Family C Tools User Guide	From Dist. through SAP	ADSP-21XX-CTOOLML	$25.00
ADSP-21000 Family C-Runtime Library Reference	From Dist. through SAP	ADSP-21XX-CRTL-ML	$10.00
ADSP-21000 SHARC Family Data Sheets			
ADSP-21060/ADSP-21060L (Rev. D)	Lit Center	C3165d-2.5-12/99	NC
ADSP-21061/ADSP-21061L (Rev. B)	Lit Center	C3244a-2.5-6/99	NC
ADSP-21062/ADSP-21062L (Rev. C)	Lit Center	C3078c-2.5-12/99	NC
ADSP-21065L (Rev. B)	Lit Center	C3533b-3-5/00	NC
ADSP-21060C/ADSP-21060LC (Rev. B)	Lit Center	C00168a-0-1/01	NC
ADSP-21160M (REV. Pr E)	Lit Center	Preliminary	NC
ADSP-21161N (REV. Pr A)	Lit Center	Preliminary	NC
ADSP-21000 SHARC Development Boards and Emulators			
ADSP-21065L EZ-LAB System Development Manual	www.analog.com/dsp	82-001916-01	NC
ADSP-2106x EZ-KIT Lite Manual	www.analog.com/dsp	82-001916-02	NC
Apex-ICE™ USB Emulator Hardware Installation Guide	www.analog.com/dsp	MANAPEXICE	NC
Trek-ICE™ Universal Emulator Hardware and Software Installation Guide	www.analog.com/dsp	MANTREKICE	NC
Mountain-ICE™ Emulator Hardware User's Guide	www.analog.com/dsp	MANMTNICE	NC
Summit-ICE™ Emulator Hardware User's Guide	www.analog.com/dsp	MANSUMICE	NC
VisualDSP Emulation Tools Installation Guide for Windows 95/98/NT/2000	www.analog.com/dsp	MANVDSPMU	NC
VisualDSP++ SHARC DSP Tools Release 1.0 Manuals			
Complete Set of ADSP-21xx VDSP Manuals - includes the following:	From Dist. through SAP	VDSP-SHARC-MAN-FULL	$100.00
VisualDSP++ Getting Started Guide			
VisualDSP++ User's Guide for the ADSP-21xxx Family DSPs			
Assembler Manual for the ADSP-21xxx Family DSPs			
C/C++ Compiler & Library Manual for the ADSP-21xxx Family DSPs			
Linker & Utilities for the ADSP-21xxx Family DSPs			
Product Bulletin for VisualDSP++ and the ADSP-21xxx Family DSPs			

http://www.analog.com/dsp/tech_doc

DSP Customer Support

Web

You can visit Analog Devices' **World Wide Web** home page. Browse through a wide assortment of information about the company and products. You can also get detailed technical information as well as cross reference information. A search engine and site map will help you find what you are looking for. You can reach Analog Devices over the internet at **www.analog.com/dsp**. Here you'll find:

- Applications and Solutions
- Development Tools
- Data Sheets & Manuals
- DSP Collaborative
- Technical Support
- University Program
- Training and Education

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You can get 24 hour access to data sheets for Analog Devices products by using the Analog Devices FAXback automated literature delivery system. Simply call **1-800-446-6212** and follow the recorded instructions. By providing a FAX code and your FAX number, you can receive a copy of a data sheet in a matter of minutes. An index of products and FAX codes can be faxed to you upon demand.

DSP Customer Support

Literature

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Faxback ++49 87 6593 00

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Web: http://www.analog.com/dsp/tools

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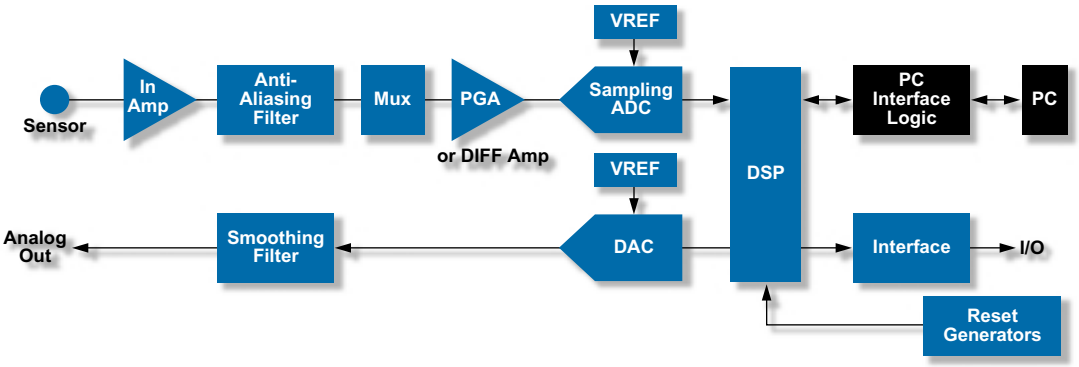
Remember …

Analog Devices Offers Products and Solutions for the Entire Signal Chain



Sensors

Interface

Supervisory

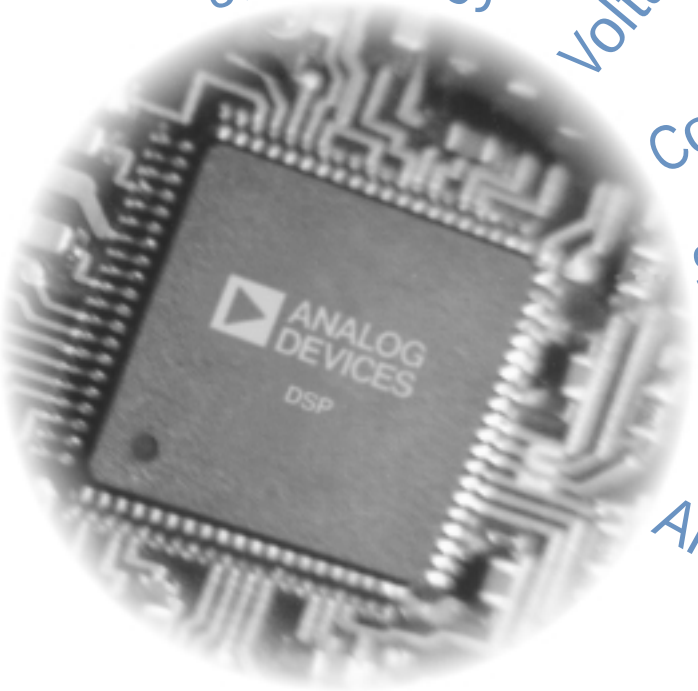
Voltage References

Converters-ADCs & DACs

Switches and Multiplexers

Power Management

Amplifiers



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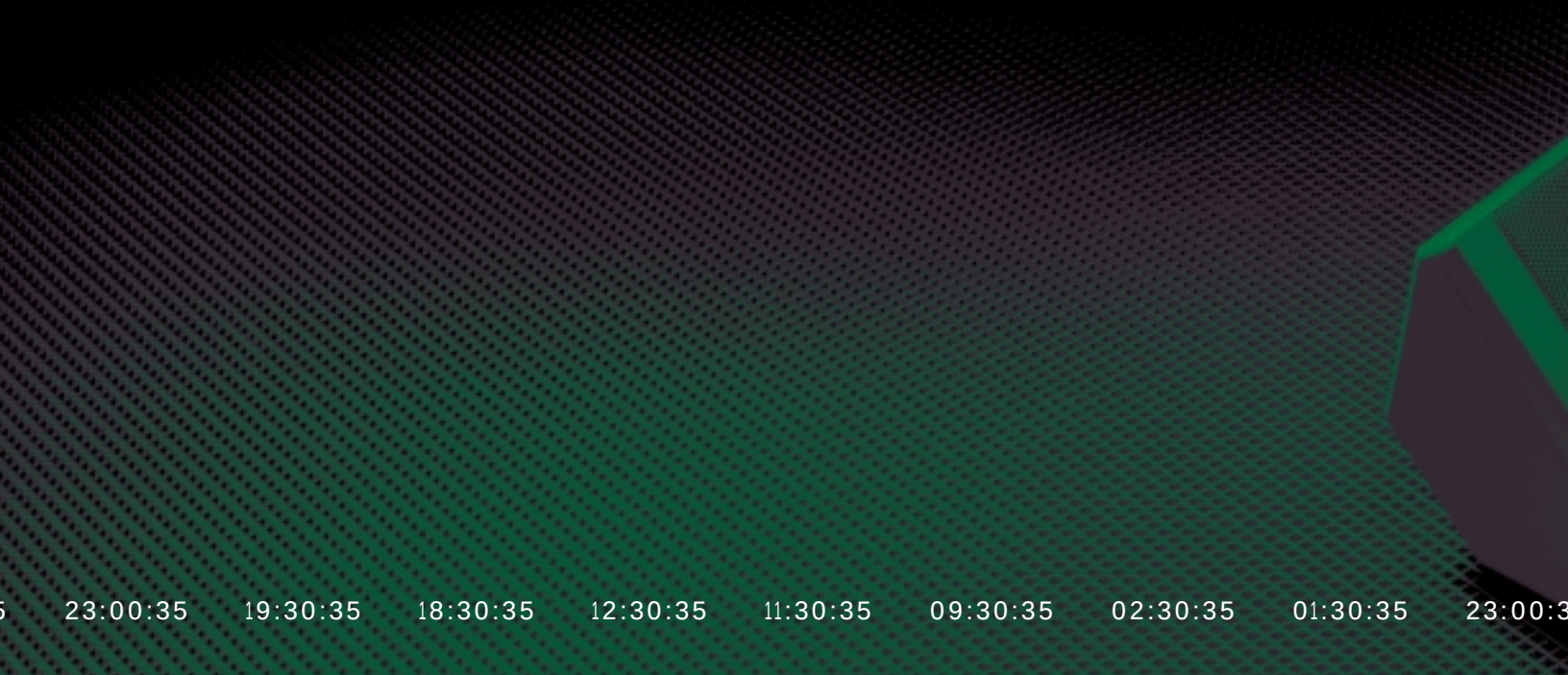

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