

I INDEX

Symbols

μ -law 5-28

Numerics

1.15 format 2-2

A

Accessing Peripherals 8-24

ADCs

interface

parallel 10-2, 10-9, 10-10, 10-38–10-39

serial 10-34–10-37

memory-mapped, reading data from 10-2–10-10

Address generators 1-15

Address latch cycle 9-33–9-34

Addresses

base, calculating 4-6

BDMA, external 9-7

next, select logic for 3-3

vector

ADSP-218x interrupt 3-16

Addressing

direct 1-16

indirect 1-16, 4-4

linear indirect addressing 4-4

modulo (circular buffers) 4-5

ADSP-2181 and ADSP-2183

pins, descriptions 7-4–7-7

A-law 5-28

ALU

arithmetic 2-3

block diagram 2-8

carry (AC) 2-38

divide primitives 2-14–2-20

division 2-14–2-20

input/output registers 2-12

multiprecision operations 2-13

overflow latch mode 2-14

overflows 2-13

registers

 ASTAT 2-9

 AX 2-9

 MSTAT 1-15, 2-10

saturation mode 2-13

standard functions 2-11

status 2-20

structure 2-8

INDEX

- Analog front ends, interfacing
 - 10-25–10-29
- AR register 2-13
- Architecture
 - core 1-12–1-16
 - Harvard, modified 8-1, 8-5
- Arithmetic
 - formats 2-5
 - Shifter 2-4
- Arithmetic Logic Unit, *see* ALU
- Arithmetic Status register (ASTAT)
 - 3-27–3-28
 - see also* ASTAT register
- Arrays and variables 4-9
- ASTAT register 2-9, B-17
- Autobuffering 5-32–5-37
 - enabled 5-53
 - example 5-36
 - service, SPORTs 5-51
 - SPORTs
 - circular buffer 5-32
 - overlay registers 5-35
 - synchronization, to processor
 - clock 5-49
- AX registers
 - AX0 2-9
 - AX1 2-9
- B**
- Barrel Shifter, *see* Shifter
- Base address, calculating 4-6
- BDMA
 - accesses, Host Mode 8-25
 - addresses, external 9-7
 - booting 9-15
 - register values 7-30
 - sequence 9-18
 - software features 9-20
 - control registers 9-5–9-13
 - controller 1-18
 - port 1-9, 9-2–9-20
 - during powerdown 7-53
 - functional description 9-4
 - transfers
 - control registers 9-5
 - formulas for 9-4
- BDMA Control register B-12, B-13
- BDMA External Address register 9-7, B-15
- BDMA Internal Address register 9-3, 9-5, 9-6, B-15
- BDMA Word Count register 9-11, B-14
- Biased rounding 2-31
- Binary
 - multiplication A-5–A-8
 - string 2-1
 - unsigned numbers 2-2
- Bit-reverse addressing 4-8
- Block floating-point format A-7–A-8
- BMODE pin 9-15
- BMS
 - disable control bit 8-21
 - see also* Byte Memory, space
- BMWAIT field 9-12, 9-13
- Boot code, generating 10-51–10-57

- Boot loading 9-46–9-47, 10-49–10-57
- Booting
 - BDMA 7-30, 9-15
 - sequence 9-18
 - IDMA 10-49–10-57
 - methods 9-16
 - ADSP-2181 and ADSP-2183 9-16
- Buffers
 - circular 4-10, 5-32
- Bus Grant Hung (BGH)
 - output 7-61
- Bus request or grant 7-59
- Buses 1-16
 - DMA 1-16, 8-2, 8-12
 - DMD 1-16, 2-9, 2-10, 2-14, 2-22, 2-23, 2-28, 2-33, 8-2
 - memory 8-2
 - PMA 1-16, 8-2, 8-9
 - PMD 1-16, 2-9, 2-22, 8-2
 - R 1-16, 2-9, 2-10, 2-22, 2-23, 2-28, 2-33
- Byte Direct Memory Access, *see* BDMA
- Byte Memory 9-2
 - interface 8-15–8-16
 - space 1-18, 8-2
 - storage formats 9-14
 - word formats 9-14
- C
- C Compiler and Assembler 1-20
- Calculating, base address 4-6
- CALL instruction 3-13
- Capacitors
 - decoupling 7-66
- Circular buffers 4-10
- Clock
 - 1/2x considerations 7-22
 - signals 7-19–7-22
 - CLKIN pin 7-19
 - CLKOUT pin 7-19
 - crystal connections 7-20
 - processor states 7-21
 - XTAL pin 7-19
 - synchronization delay 7-22
- CMS, *see* Composite Memory Select 8-3
- Code
 - boot 10-51–10-57
 - host 10-52–10-57
- Codecs
 - interface, serial 10-32
 - interfacing 10-25–10-29
- Common-mode pins 7-9–7-12
- Companding
 - delay, SPORTs 5-44
 - operation example 5-29
 - receive
 - example 5-52
 - latencies 5-52

INDEX

- SPORTs 5-28–5-31
 - A-law and μ -law 5-28
 - hardware contention 5-30
 - internal data 5-31
 - operation sequence 5-29
- Composite Memory Select (CMS) 8-18–8-22
- Composite Memory Select register (CMS) 8-3
- Composite Select Control register 9-12, 9-13, B-11
- Computational units 1-14, 2-1–2-49
 - ALU 2-3, 2-7
 - MAC 2-4
 - overview 2-1
 - Shifter 2-4
- Conditional instructions 3-33
- Configuration
 - SPORTs, example 5-19
- Configuring interrupts 3-19–3-25
- Contention
 - companding hardware, SPORTs 5-30
- Conventions, document 1-25
- Core architecture 1-12–1-16
- Customer support 1-24
- Cycle
 - address latch 9-25, 9-33–9-34
 - long read 9-35–9-37
 - long write 9-41–9-44
 - overlay latch 9-34
 - short read 9-37–9-39
 - short read only mode 9-40–9-41
 - short write 9-44–9-46
 - stealing 9-1, 9-47
- D
- DACs
 - interface, serial 10-40
 - memory-mapped, writing data to 10-10–10-16
- Data
 - accesses, programming 4-9
 - format, SPORTs 5-28–5-31
- Data address generators (DAGs)
 - 4-1–4-13
 - block diagram 4-2
 - overview 4-1
 - registers 4-2
 - using with hardware overlays 4-14
- Data Memory 8-1
 - interface 8-12–8-15
 - overlays 8-12–8-15
- Data Memory Address bus, *see* DMA bus
- Data Memory Data bus, *see* DMD bus
- Data Memory Overlay register (DMOVLAY) 8-12–8-15
 - using with autobuffering 4-14, 5-35
 - using with DAGs 4-14, 5-35
- Debugger 1-20
- Delay, clock synchronization 7-22
- Denormalize 2-44
- Derive block exponent instruction 2-41

- Development tools [1-19–1-23](#)
 - Diodes, protection [7-36](#)
 - Direct addressing [1-16](#)
 - Divide primitives, ALU [2-14–2-20](#)
 - DIVQ [2-17–2-20](#)
 - DIVS [2-14–2-17](#)
 - Division, ALU [2-14–2-20](#)
 - DIVQ [2-17–2-20](#)
 - DIVS [2-14–2-17](#)
 - DMA bus [1-16, 8-2, 8-12](#)
 - DMA ports [1-18](#)
 - DMD bus [1-16, 2-9, 2-10, 2-14, 2-22, 2-23, 2-28, 2-33, 8-2](#)
 - DO UNTIL instruction [3-6–3-10](#)
 - termination condition logic [3-7](#)
 - DO UNTIL loops [3-13](#)
 - Document, conventions [1-25](#)
 - Documents, related [1-24](#)
 - DSPs
 - interfacing to [10-1–10-32](#)
 - multiple [10-58](#)
 - performance [1-11](#)
 - see also* Processors
 - DTYPE field, SPORT Control
 - register [5-28](#)
 - Dual power supply, M series
 - processors [7-39](#)
- E**
- Emulation, EZ_ICE [7-68](#)
 - ERESET signal, with Mode pins [7-64](#)
 - ESD protection [7-36](#)
 - Examples, interfacing [10-32–10-59](#)
- External
 - interrupts [7-31–7-33](#)
 - memory spaces [8-3](#)
 - Overlay Memory [8-3](#)
 - Program Memory [8-9](#)
 - TTL/CMOS clock [7-48](#)
 - EZ-ICE [1-22](#)
 - bus request signal [7-65](#)
 - circuit for ADSP-218x Mode pins [7-65](#)
 - connector [7-63](#)
 - emulation [7-68](#)
 - memory select signal with [7-66](#)
 - powerup procedure [7-68](#)
 - probe, target system board
 - connector [7-62](#)
 - EZ-KIT Lite [1-21](#)
- F**
- Flag pins [7-33–7-35](#)
 - during powerdown [7-51](#)
 - general purpose [7-34](#)
 - Floating-point, block format [A-7–A-8](#)
 - Formats
 - arithmetic [2-5](#)
 - block floating-point [A-7–A-8](#)
 - fractional [A-2–A-4](#)
 - integer [A-2–A-4](#)
 - twos-complement [A-1](#)
 - Fractional
 - format [A-2–A-4](#)
 - mode [A-6](#)
 - representation: 1.15 [2-2](#)

INDEX

- Frame
 - synchronization 5-2, 5-14
 - internally generated 5-45
 - signal 5-2, 5-17, 5-18, 5-27
 - signal source 5-15–5-16
- Framing mode, normal and alternate 5-21–5-27
- Full Memory Mode 1-9, 8-23
 - pins 7-12, 8-26
- Functional units 1-6–1-8
- Functions
 - ALU 2-11
 - MAC 2-24
- G**
- Gated serial clocks 5-55
- Generators, reset 7-40–7-42
- Global enable/disable for interrupts 3-23
- Go mode 3-32
 - bus request or grant 7-59
- H**
- Hardware
 - development tools 1-21
 - host interface design 10-45–10-48
 - signaling 10-59
 - target system 7-62–7-70
- Harvard architecture, modified 8-1, 8-5
- Hold offs 9-47
- Host
 - code, generating 10-52–10-57
 - interface, hardware design 10-45–10-48
 - message transfers 10-57
- Host Memory Mode 1-9, 8-24–8-26
 - pins 7-13, 8-26
- I**
- I/O Memory
 - space 8-2, 8-16–8-18
- I/O ports
 - interfacing 10-25–10-29
- IACK acknowledge 9-47
- ICNTL register 3-20, B-17
- IDLE instruction 3-15
- IDMA
 - address latch cycle 9-25
 - timing 9-33
 - booting 10-49–10-57
 - control register, modifying 9-31
 - interface 10-42–10-59
 - long read cycle 9-35–9-37
 - timing 9-36
 - long write cycle 9-41–9-44

- port 1-9, 8-4, 9-21–9-50
 - boot loading 9-46–9-47, 10-49–10-57
 - during powerdown 7-53
 - functional description 9-28–9-31
 - input signals 9-23
 - interface 9-21
 - pins 9-22
- short read cycle 9-37–9-39
 - short read only mode timing 9-40
 - timing 9-38, 9-40
- short read only mode cycle 9-40–9-41
- short write cycle 9-44–9-46
 - timing 9-45
- system design issues 10-49–10-57
- timing 9-32–9-41
- transfers 9-28–9-31
 - sequence 10-43
- IDMA Control register 9-24–9-30, 10-44, B-16
- IDMA Overlay register 9-24–9-26, B-16
 - Overlay latch cycle 9-34
 - Short Read Only mode 9-41
 - short read only mode 9-41
- IF conditions logic 3-33
- IFC register 3-23, B-18
- IMASK register 3-20, B-18
- ISRs 3-21
- Immediate shifts 2-42
- Indirect addressing 1-16, 4-4
- Input formats 2-27
- Instruction set 1-10
- Instructions
 - CALL 3-13
 - completion latencies 5-50
 - conditional 3-33
 - DO UNTIL 3-6–3-10
 - termination condition logic 3-7
 - IDLE 3-15
 - JUMP 3-11
 - Mode Control 3-30
 - program control 3-11–3-16
 - slow IDLE 3-15
 - status conditions 3-33
 - TOPPCSTACK 3-34
 - registers used 3-35
 - restrictions 3-37
- Integer
 - format A-2–A-4
 - mode A-6
- Integrated development environment (IDE) 1-19
- Interfaces
 - Byte Memory 8-15–8-16
 - Data Memory 8-12–8-15
 - host 10-45–10-48
 - IDMA 10-42–10-59
 - memory 1-9
 - memory mappings 8-5–8-9
 - Program Memory 8-9–8-12
 - system 1-9

INDEX

- Interfacing
 - analog front ends [10-25–10-29](#)
 - codecs [10-25–10-29](#)
 - examples [10-32–10-59](#)
 - high-speed [10-29–10-32](#)
 - I/O Ports [10-25–10-29](#)
 - parallel [10-2–10-16](#)
 - serial [10-16–10-25](#)
 - to DSPs [10-1–10-32](#)
 - Internal Direct Memory Access, *see*
 - IDMA
 - Interrupt Control register, *see*
 - ICNTL register
 - Interrupt Force and Clear register,
see IFC register
 - Interrupt Mask register, *see* IMASK
register
 - Interrupts
 - autobuffering enabled [5-53](#)
 - configuring [3-19–3-25](#)
 - external [7-31–7-33](#)
 - global enable/disable [3-23](#)
 - latency [3-24](#)
 - non-maskable
 - using powerdown as [7-59](#)
 - processor operation during
 - powerdown [7-51](#)
 - program sequencer [3-16–3-25](#)
 - receive timing [5-48](#)
 - sensitivity [7-32](#)
 - servicing sequence [3-18](#)
 - SPORTs [5-5](#)
 - priorities [5-5](#)
 - synchronization to processor clock [5-49](#)
 - transmit timing [5-47](#)
 - vector addresses [3-16](#)
 - INVRFS bit, SPORT Control
register [5-19](#)
 - INVTFS bit, SPORT Control
register [5-19](#)
 - IO pin, ESD protection [7-36](#)
 - IRFS bit, SPORT Control register
[5-15](#)
 - ISCLK bit, SPORT Control register
[5-11, 5-12](#)
 - ITFS bit, SPORT Control register
[5-15](#)
- ## J
- JUMP instruction [3-11](#)
 - direct [3-11](#)
 - register indirect
overlays [4-14](#)
- ## L
- Latch
 - IDMA address timing [9-33](#)
 - Latencies
 - instruction completion [5-50](#)
 - receive companding [5-52](#)
 - Latency, interrupts [3-24](#)
 - Linear indirect addressing [4-4](#)
 - Linker [1-21](#)
 - Linker Description File [1-21](#)
 - Loader [1-21](#)

- Loop comparator and stack 3-6–3-10
- Loop counter register and stack 3-5
- Loops
 - DO UNTIL 3-13
- M
- MAC 2-20–2-32
 - arithmetic 2-4
 - input/output registers 2-28
 - operations 2-24
 - overflow and saturation 2-29
 - standard functions 2-24
 - structure 2-21
- Memory
 - architecture
 - ADSP-2181, ADSP-2183, and ADSP-2185 8-6
 - ADSP-2184 8-6
 - ADSP-2186 8-7
 - ADSP-2187L 8-7
 - ADSP-2188M 8-8
 - ADSP-2189M 8-8
 - buses 8-2
 - byte 9-2
 - Data 8-1
 - external 8-1, 8-2
 - external overlay 8-3
 - interface
 - modes 8-23–8-27
 - pins 8-26
 - interfaces 8-1–8-27
 - interfaces, mappings 8-5–8-9
 - mode pins 7-12–7-13
 - modes 8-4
 - Program 8-1
 - select signals 7-66
 - spaces
 - Byte 1-18, 8-2
 - external 8-3
 - I/O 8-2
- Memory interface 1-9
- Memory select signals
 - PMS, DMS, BMS, and IOMS 8-19
- Memory-Mapped registers B-3–B-16
- MMAP pin 9-15
- Mode
 - active or passive pin configuration 7-13
 - framing, normal and alternate 5-21–5-27
 - multichannel 5-38
 - pins 8-26
 - multiplexing 8-4
 - with RESET and ERESET signals 7-64
 - single-channel 5-38
- Mode A pin 9-15
- Mode B pin 9-15
- Mode C pin 8-23, 8-24, 9-15
- Mode Control instructions 3-30
- Mode D pin 9-15
- Mode Status register (MSTAT), *see* MSTAT

INDEX

Modes

- fractional [A-6](#)
- Go [3-32](#)
- integer [A-6](#)
- memory [8-4](#)
 - Full Memory [1-9, 8-23](#)
 - Host Memory [1-9, 8-24–8-26](#)
 - interface [8-23–8-27](#)

Modulo addressing (circular buffers) [4-5](#)

Monitors

- power supply [7-42](#)

MR register

- operation [2-28](#)

MSTAT register [1-15, 2-10, 2-13, 2-14, 3-30, B-17](#)

- secondary set [3-31](#)

Multichannel function

- SPORTs [5-38–5-43](#)
 - setup [5-39](#)

Multiple processors [10-58](#)

Multiplication

- binary [A-5–A-8](#)

Multiplier/Accumulator, *see* MAC

Multiprecision operation, ALU [2-13](#)

N

Next address select logic [3-3](#)

Non-Memory Mapped registers [B-17–B-18](#)

Normalize [2-45](#)

Numbers

- binary [2-1](#)
- fractional format: 1.15 [2-2](#)
- signed [2-2, A-1](#)
- unsigned [A-1](#)
- unsigned binary [2-2](#)

O

On-chip peripherals [1-17–1-18](#)

Overflow latch mode, ALU [2-14](#)

Overflows, ALU [2-13](#)

Overlay latch cycle [9-34](#)

Overlays

- Data Memory [8-12–8-15](#)
- memory, external [8-3](#)
- Program Memory [8-9, 8-10](#)
 - internal and external [8-11](#)
 - using autobuffering with [5-35](#)
 - using DAGs with [4-14, 5-35](#)

Overshoot and ringing

- SPORTs [5-57](#)

P

Packages

- 100-LQFP [7-7–7-14](#)
 - common-mode pins [7-9–7-12](#)
 - memory mode pins [7-12–7-14](#)
- 128-LQFP [7-3–7-7](#)
- processor configurations [7-1](#)

Parallel

- interface [10-2, 10-9, 10-10](#)
- interfacing to DSPs [10-2–10-16](#)
- port, ADC interface [10-38–10-39](#)

- PC stack
 - popping top value [3-34](#)
 - pushing top value [3-34](#)
- PCB board
 - target systems [7-67](#)
- Performance, DSP [1-11](#)
- Peripherals, on-chip [1-17–1-18](#)
- Pins
 - 100-LQFP packages
 - common-mode [7-9–7-12](#)
 - memory mode [7-12–7-14](#)
 - active or passive mode
 - configuration [7-13](#)
 - BMODE [9-15](#)
 - Bus Grant Hung (BGH) [7-61](#)
 - CLKIN [7-19](#)
 - CLKOUT [7-19](#)
 - common-mode [7-9–7-12](#)
 - descriptions [7-1–7-19](#)
 - 100-LQFP packages [7-7–7-14](#)
 - 128-LQFP packages [7-3–7-7](#)
 - ADSP-2181 and ADSP-2183 [7-4–7-7](#)
 - flag [7-33–7-35](#)
 - general purpose [7-34](#)
 - Full Memory Mode [7-12, 8-26](#)
 - Host Memory Mode [7-13, 8-26](#)
 - IDMA port [9-22](#)
 - memory interface [8-26](#)
 - memory mode [7-12–7-13](#)
 - MMAP [9-15](#)
- Mode
 - EZ-ICE circuit for [7-65](#)
 - with RESET and ERESET signals [7-64](#)
 - Mode A [9-15](#)
 - Mode B [9-15](#)
 - Mode C [9-15](#)
 - Mode D [9-15](#)
 - powerdown and acknowledge (PWDACK) [7-57](#)
 - states during powerdown [7-54–7-57](#)
 - unused
 - recommendations [7-18](#)
 - terminating [7-14](#)
 - XTAL [7-19](#)
- PMA bus [1-16, 8-2, 8-9](#)
- PMD bus [1-16, 2-9, 2-22, 8-2](#)
- PMD-DMD bus exchange [1-16, 2-9, 2-22, 4-11](#)
 - block diagram [4-12](#)
 - structure [4-11–4-13](#)
- Ports
 - BDMA [1-9, 9-2–9-20, 9-21](#)
 - IDMA [8-4, 9-21–9-50](#)
 - functional description [9-28–9-31](#)
 - parallel
 - ADC interface [10-38–10-39](#)
 - serial [1-17](#)
 - ADC interface [10-34–10-37](#)
 - codec interface [10-32](#)
 - DAC interface [10-40](#)

INDEX

- Power
 - consumption, lowest 7-54–7-57
 - supplies
 - dual, for M series processors 7-39
 - dual-voltage processors 7-37
 - monitor for 7-42
- Powerdown 7-43–7-58
 - BDMA port during 7-53
 - control 7-44
 - entering 7-45
 - exiting 7-46
 - with the Powerdown pin 7-46
 - with the RESET pin 7-47
 - IDMA port during 7-53
 - pin states during 7-54–7-57
 - powerdown and acknowledge pin (PWDACK) 7-57
 - processor operation during 7-51
 - interrupts and flags 7-51
 - SPORTs 7-51
 - sequence 7-45
 - startup time after 7-48
 - timing examples 7-58
 - using as a non-maskable interrupt 7-59
- Powerdown pin (PWD)
 - exiting with 7-46
- Powerup
 - dual-voltage processors 7-35–7-39
 - EZ-ICE 7-68
 - sequence
 - dual voltage processors 7-36
- Priority chain 9-49
- Processors
 - ADSP-218x family 1-4–1-6, C-1
 - after reset or software reboot 7-25–7-29
 - package configurations 7-1
 - resetting 7-23–7-29
- Products, third party 1-22
- Program control instructions 3-11–3-16
- Program Memory 8-1
 - external 8-9
 - interface 8-9–8-12
 - Overlay regions 8-11
 - Overlay segments 8-9, 8-10
- Program Memory Address bus, *see* PMA bus
- Program Memory Data bus, *see* PMD bus
- Program Memory Overlay register (PMOVLAY) 8-9, 8-10
 - using with autobuffering 4-14, 5-35
 - using with DAGs 4-14, 5-35
- Program sequencer 1-15, 3-1–3-38
 - interrupts 3-16–3-25
 - overview 3-1
 - structure 3-2
- Programmable Flag and Composite Select Control register 7-34, 8-15, B-11
- Programmable Flag Data register 7-35, B-12
- Programming data accesses 4-9
- PX register 4-12

R

R bus 1-16, 2-9, 2-10, 2-22, 2-23,
2-28, 2-33

Rebooting

software-forced 7-24

Rebooting, timer during 7-25

Receive

companding example 5-52

interrupt timing 5-48

References

hardware interface design 10-59

Registers

ADSP-218x B-2

ALU 2-9

input/output 2-12

AR 2-13

Arithmetic Status register

(ASTAT) 2-9, 3-27–3-28, B-17

BDMA Control 9-5–9-13, B-12,
B-13

BDMA External Address 9-7,
B-15

BDMA Internal Address 9-3, 9-5,
9-6, B-15

BDMA Word Count B-14

Composite Memory Select (CMS)
8-3

Composite Select Control B-11

data address generators 4-2

Data Memory Overlay

(DMOVLAY) 8-12–8-15

ICNTL 3-20

IDMA Control 9-24–9-30,
10-44, B-16

modifying 9-31

IDMA Overlay 9-24–9-26, B-16

IFC 3-23

IMASK 3-20

ISRs 3-21

Interrupt Control (ICNTL) B-17

Interrupt Force and Clear (IFC)
B-18

Interrupt Mask (IMASK) B-18

loop counter 3-5

MAC input/output 2-28

Memory-Mapped B-3–B-16

Mode Status (MSTAT) 1-15,
2-10, 2-13, 2-14, 3-30, B-17
secondary set 3-31

Non-Memory Mapped B-17–
B-18

Program Memory Overlay
(PMOVLAY) 8-9, 8-10

Programmable Flag and
Composite Select Control 7-34,
8-15, B-11

Programmable Flag Data 7-35,
B-12

PX 4-12

secondary set 3-31

SPORT Autobuffer Control 5-34

SPORT Control

DTYPE field 5-28

SLEN field 5-13

SPORT0 Autobuffer Control B-7

INDEX

- SPORT0 Control [B-5](#)
- SPORT0 Multichannel Word
 - Enable [B-6](#)
- SPORT0 RFS DIV [B-7](#)
- SPORT0 SCLK DIV [B-7](#)
- SPORT1 Autobuffer Control
 - [B-10](#)
- SPORT1 Autobuffer/Powerdown Control [7-44](#)
- SPORT1 Control [B-8](#)
- SPORT1 RFS DIV [B-9](#)
- SPORT1 SCLK DIV [B-9](#)
- SPORTs
 - configuration [5-6](#)
 - receive (RX0 and RX1) [5-9](#)
 - transmit (TX0 and TX1) [5-9](#)
- Stack Status (SSTAT) [3-28](#), [B-17](#)
- status [3-26](#)
 - ASTAT [3-27](#)
 - MSTAT [3-30](#)
 - SSTAT [3-28](#)
- System Control [5-10](#), [B-3](#)
- timer [B-5](#)
 - period [6-1](#)
 - TCOUNT [6-2–6-6](#)
 - TPERIOD [6-2–6-6](#)
 - TSCALE [6-2–6-6](#)
- values
 - BDMA booting [7-30](#)
- Wait State Control [8-16–8-17](#), [B-4](#)
- Related documents [1-24](#)
- Requests
 - priority chain for concurrent [9-49](#)
- RESET
 - pin, exiting with [7-47](#)
 - signal
 - target systems [7-67](#)
 - with Mode pins [7-64](#)
- Reset
 - generators [7-40–7-42](#)
 - for M series processors [7-41](#)
 - processor [7-23–7-29](#)
- Result bus, *see* R bus
- RFSR bit, SPORT Control register
 - [5-14](#)
- RFSW bit, SPORT Control register
 - [5-18](#)
- Rounding mode [2-30](#)
- S
- Saturation mode
 - ALU [2-13](#)
- Serial
 - ADC
 - to DSP Interface [10-19–10-22](#)
 - DAC
 - to DSP Interface [10-23–10-25](#)
 - interfacing to DSPs [10-16–10-25](#)
 - port
 - ADC interface [10-34–10-37](#)
 - codec Interface [10-32](#)
 - DAC interface [10-40](#)
- Serial clocks [5-11–5-57](#)
 - frequencies [5-12](#)
 - gated [5-55](#)
 - signal [5-11](#)
- Serial Ports, *see* SPORTs

- Shifter 2-4, 2-32–2-49
 - arithmetic 2-4
 - input/output registers 2-41
 - operations 2-40
 - structure 2-32
- Signal
 - Composite Memory Select (CMS) 8-18–8-22
- Signaling
 - hardware 10-59
- Signals
 - bus request (BR), with EZ-ICE 7-65
 - clock 7-19–7-22
 - frame synchronization 5-2
 - IDMA port, input 9-23
 - memory select 7-66, 8-19
 - RESET
 - target systems 7-67
 - SCLK 5-11
- Signed numbers A-1
 - twos- complement 2-2
- SLEN field 5-13
- Slow IDLE instruction 3-15
- Software
 - development tools 1-20–1-21
 - forced rebooting 7-24
- Space
 - I/O Memory 8-16–8-18
- SPORT Control register
 - ISCLK bit 5-11, 5-12
 - SLEN field 5-13
- SPORT0 Autobuffer Control
 - register B-7
- SPORT0 Control register B-5
- SPORT0 Multichannel Word
 - Enable registers B-6
- SPORT0 RFS DIV register B-7
- SPORT0 SCLK DIV register B-7
- SPORT1
 - configuration 5-10
 - Flag In (F1) and Flag Out (FO) pins 7-33
- SPORT1 Autobuffer Control
 - register B-10
- SPORT1 Autobuffer/Powerdown
 - Control register 7-44
- SPORT1 Control register B-8
- SPORT1 RFS DIV registers B-9
- SPORT1 SCLK DIV register B-9
- SPORTs 1-17, 5-1–5-55
 - Autobuffer Control register 5-34
 - autobuffering 5-32–5-37
 - circular 5-32
 - enabled 5-53
 - overlay registers 5-35
 - service 5-51
 - synchronization 5-49
 - basic description 5-1–5-6
 - block diagram 5-2
 - companding 5-28–5-31
 - A-law and μ -law 5-28
 - hardware contention 5-30
 - internal data 5-31
 - operation sequence 5-29
 - configuration 5-6–5-8
 - example 5-19
 - registers 5-6

INDEX

- data format 5-28–5-31
- enable 5-10
- external enable circuit 5-58
- interrupts 5-5
 - autobuffering enabled 5-53
 - priorities 5-5
 - service 5-51
 - synchronization to processor clock 5-49
- ISCLK bit 5-11, 5-12
- latencies
 - instruction completion 5-50
 - receive companding 5-52
- multichannel
 - function 5-38–5-43
 - setup 5-39
- operation 5-5
- overshoot and ringing 5-57
- processor operation during powerdown 7-51
- programming 5-6–5-9
- receiving and transmitting data 5-9
- registers
 - receive (RX0 and RX1) 5-9
 - transmit (TX0 and TX1) 5-9
- serial clocks 5-11–5-57
 - gated 5-55
 - signal 5-11
- SPORT Control register
 - INVTFS and INVRFS bits 5-19
 - ITFS and IRFS bits 5-15
 - RFSR and TFSR bits 5-14
 - TFSW and RFSW bits 5-18
- System Control register 5-10
- timing 5-44–5-55
 - companding delay 5-44
 - example 5-21–5-27
 - internally generated frame synchronization 5-45
 - startup 5-45
 - synchronization delay 5-44
- word
 - framing 5-14
 - length 5-13
- Stack Status register (SSTAT) 3-28, B-17
- Stacks
 - counter 3-5
 - status 3-26
- Startup
 - SPORTs, timing 5-45
 - time after powerdown 7-48
 - crystal and internal oscillator 7-49
 - external TTL/CMOS clock 7-48
- Status
 - registers 3-26
 - ASTAT 3-27
 - MSTAT 3-30
 - SSTAT 3-28
 - stack 3-26
- Status conditions
 - IF condition logic 3-33
- Synchronization delay
 - SPORTs timing 5-44

- Synchronization
 - frame 5-2, 5-14
 - internally generated 5-45
 - signal 5-17, 5-18, 5-27
 - signal source 5-15–5-16
- System Control register 5-10, B-3
- System interface 1-9, 7-1–7-70, 10-31
- T
- Target systems
 - board connector for EZ-ICE
 - probe 7-62
 - decoupling capacitors 7-66
 - hardware 7-62–7-70
 - PCB board 7-67
- Terminating, unused pins 7-14
- TFSR bit, SPORT Control register 5-14
- TFSW bit, SPORT Control register 5-18
- Third party products 1-22
- Timer 1-17, 6-1–6-7
 - architecture 6-2
 - block diagram 6-3
 - enabling 6-6
 - operation 6-4
 - period register 6-1
 - rebooting 7-25
- registers B-5
 - TCOUNT 6-2–6-6
 - TPERIOD 6-2–6-6
 - TSCALE 6-2–6-6
- resolution 6-4
- Timing
 - IDMA 9-32–9-41
 - long read cycle 9-36
 - long write cycle 9-43
 - short read cycle 9-38
 - short read cycle, short read only mode 9-40
 - short write cycle 9-45
 - receive interrupts 5-48
 - SPORTs 5-44–5-55
 - example 5-21–5-27
 - internally generated frame synchronization 5-45
 - transmit interrupts 5-47
- Tools
 - development 1-19–1-23
 - hardware development 1-21
 - software development 1-20–1-21
- TOPPCSTACK instruction 3-34
 - registers used 3-35
 - restrictions 3-37
- Transfers
 - BDMA
 - control registers 9-5
 - formulas for 9-4
 - host messages 10-57
 - IDMA 9-28–9-31, 10-43
 - Transmit interrupt timing 5-47
- Twos-complement format A-1

INDEX

U

Underflows, ALU [2-13](#)

Unsigned binary numbers [2-2](#), [A-1](#)

V

Variables and arrays [4-9](#)

W

Wait State Control register [8-16](#)–
[8-17](#), [B-4](#)

Word

framing, SPORTs [5-14](#)

length, SPORTs [5-13](#)