

A

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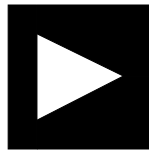
2

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ADSP-BF533 EZ-KIT Lite

DNP = Do Not Populate

		ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title		ADSP-BF533 EZ-KIT LITE - TITLE			
Size	Board No.	Rev			
C	A0167-2001	1.6C			
Date	12-21-2004_15:13	Sheet	1	of	12

Approvals	Date
Drawn	
Checked	
Engineering	

A

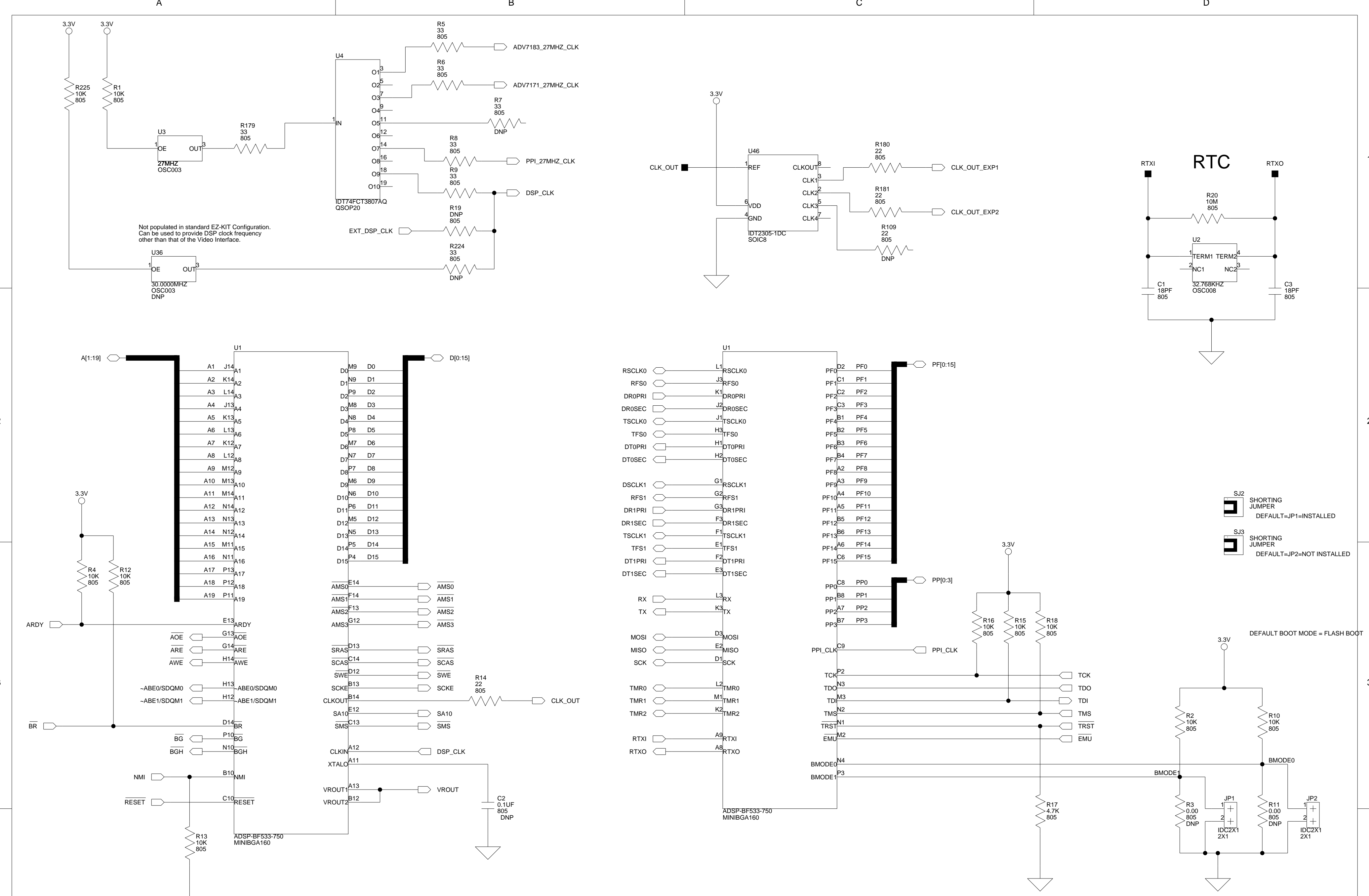
B

C

D

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4



Not populated in standard EZ-KIT Configuration.
Can be used to provide DSP clock frequency
other than that of the Video Interface.

RTC

DEFAULT BOOT MODE = FLASH BOOT

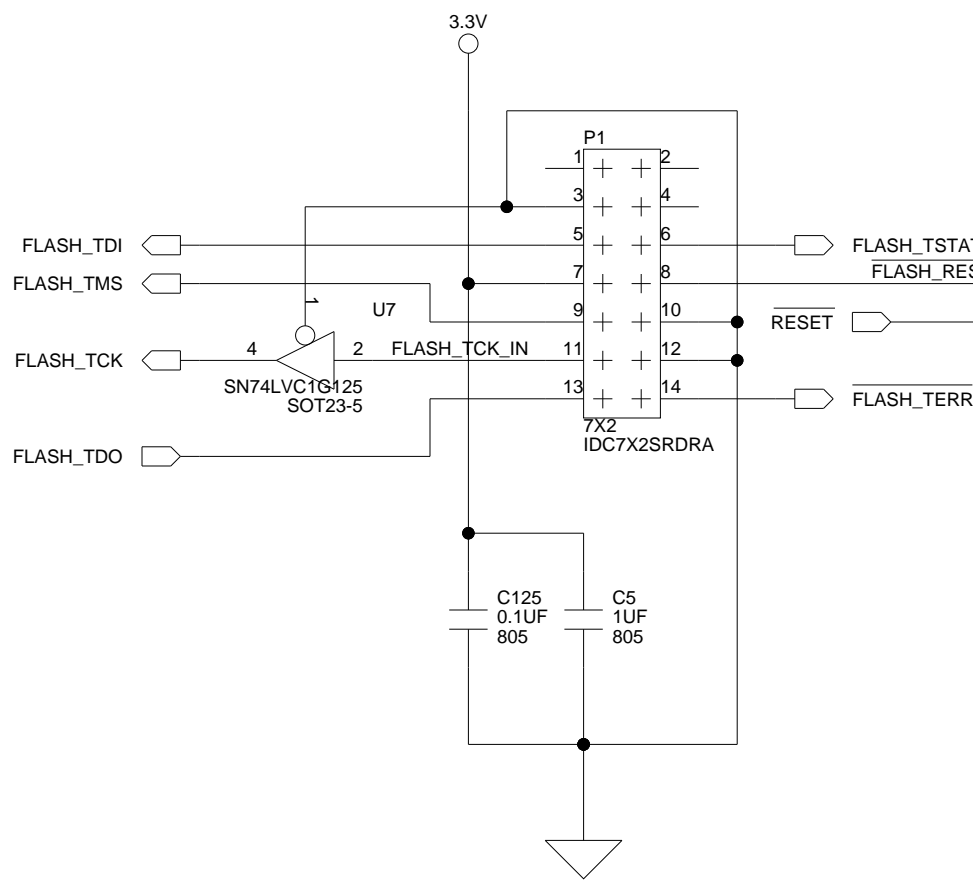
DNP = Do Not Populate



20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Approvals		Date		Title	
Drawn				ADSP-BF533 EZ-KIT LITE - DSP	
Checked				Size C	Board No. A0167-2001
Engineering				Date	Rev 1.6C
				Date	12-21-2004_15:13
				Sheet	2 of 12

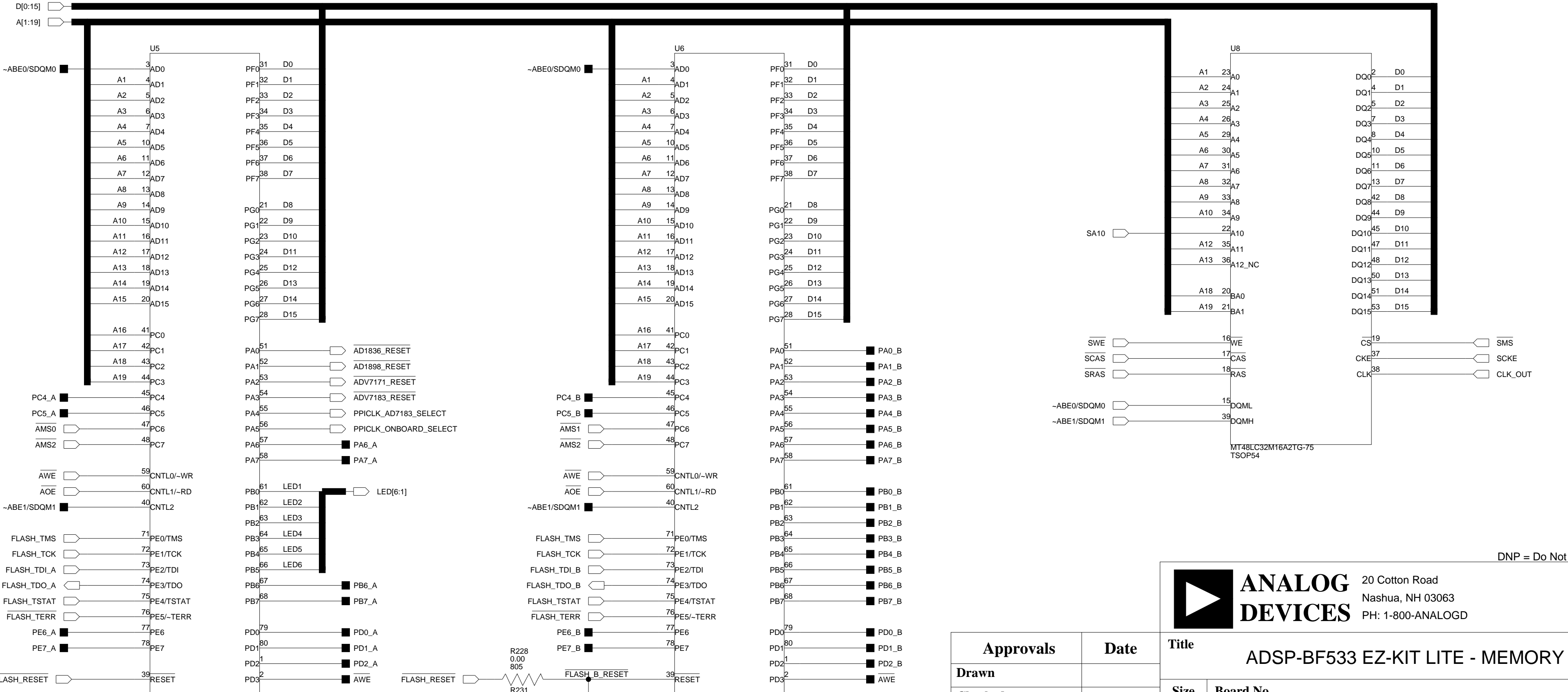
FlashLINK JTAG HEADER



FLASH A (1MB)
512K x 16

FLASH B (1MB)
512K x 16

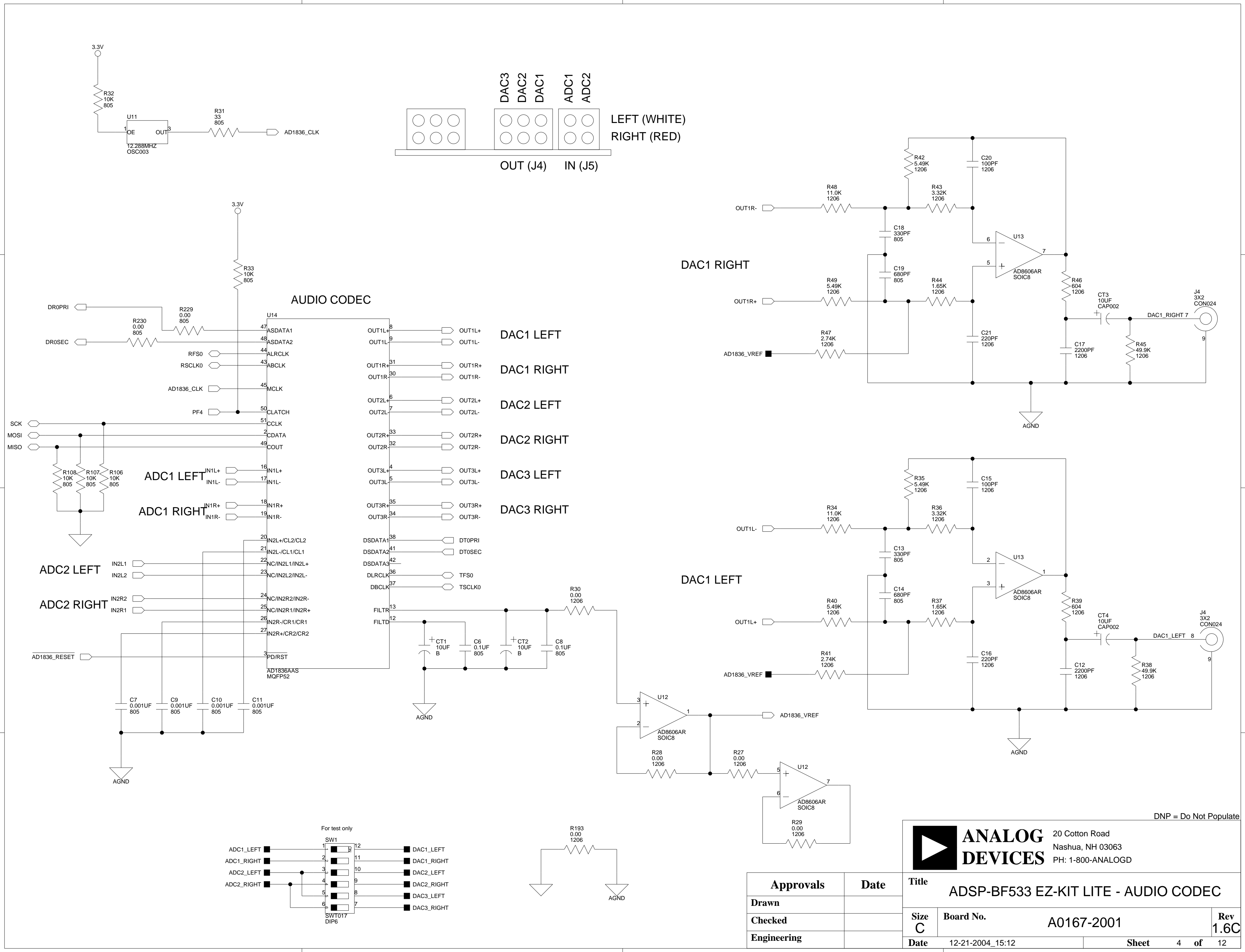
SDRAM 512Mb
(64MB - 32M x 16)



DNP = Do Not Populate



Approvals		Date		Title	
Checked		Engineering		ADSP-BF533 EZ-KIT LITE - MEMORY	
Size C	Board No.	A0167-2001		Rev	1.6C
Date	12-21-2004_15:12		Sheet	3 of 12	

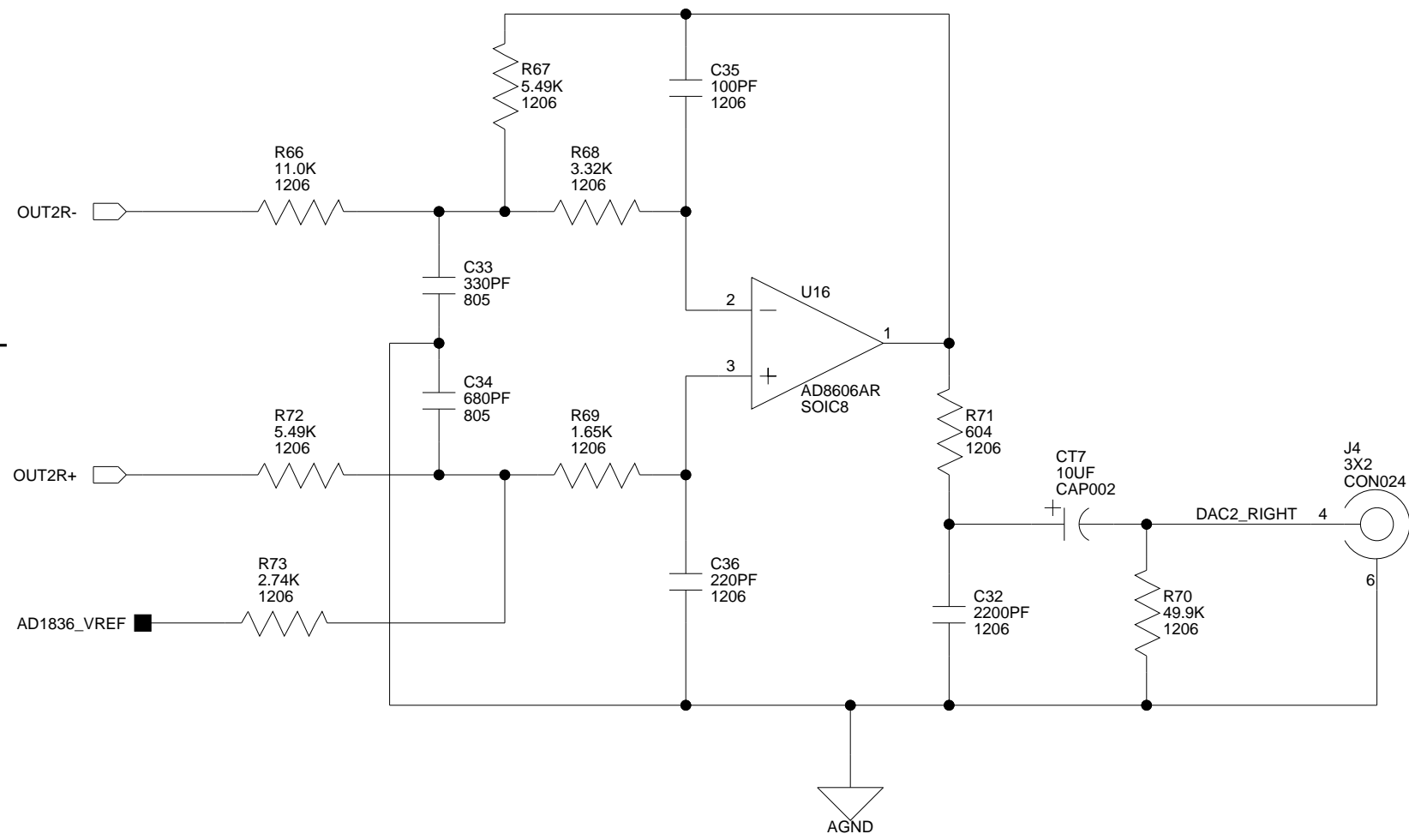


DNP = Do Not Populate

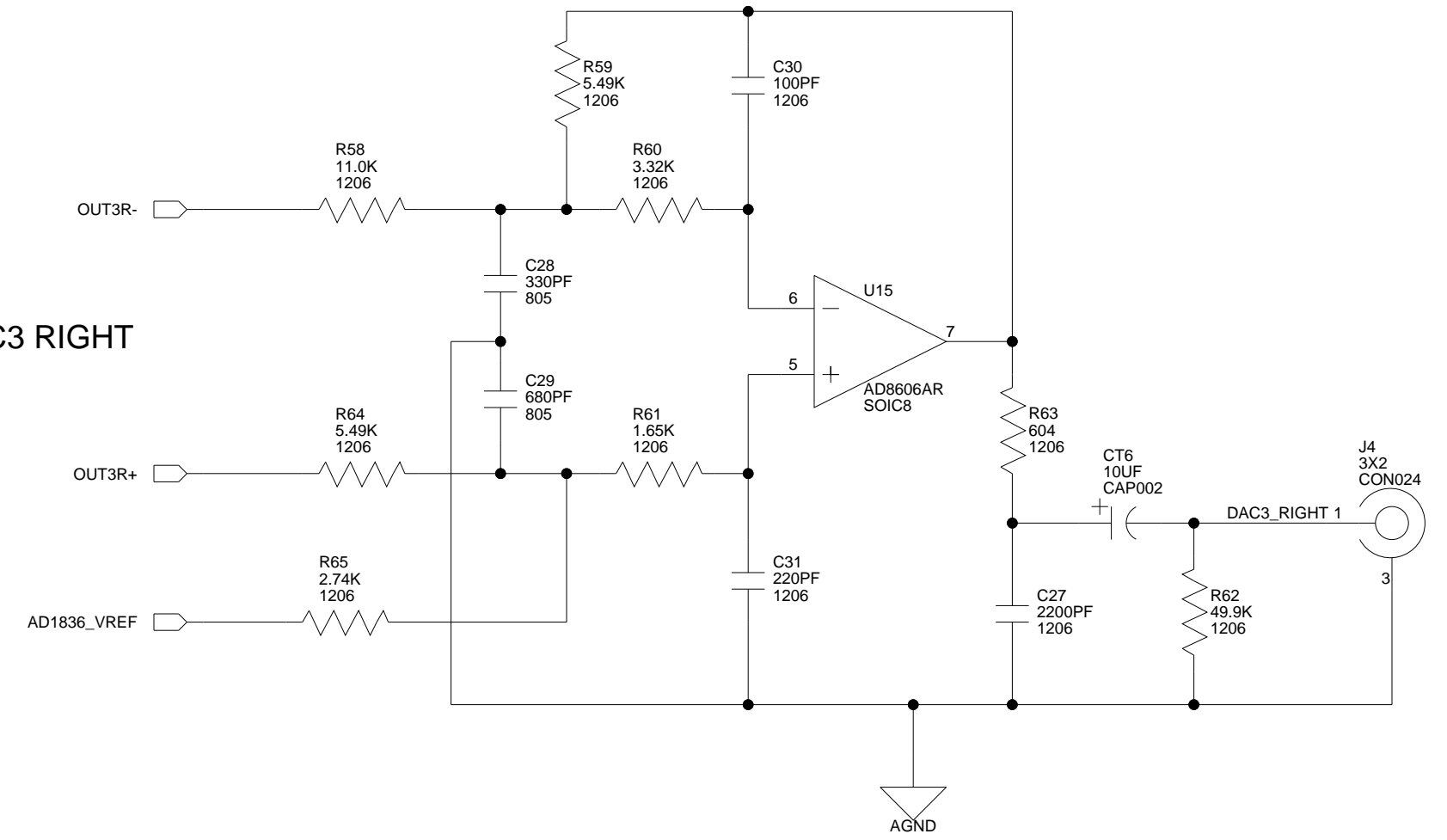
ANALOG DEVICES 20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Approvals		Date		Title ADSP-BF533 EZ-KIT LITE - AUDIO CODEC	
Drawn		Checked		Size C	Board No. A0167-2001
Engineering		Date 12-21-2004_15:12		Rev 1.6C	Sheet 4 of 12

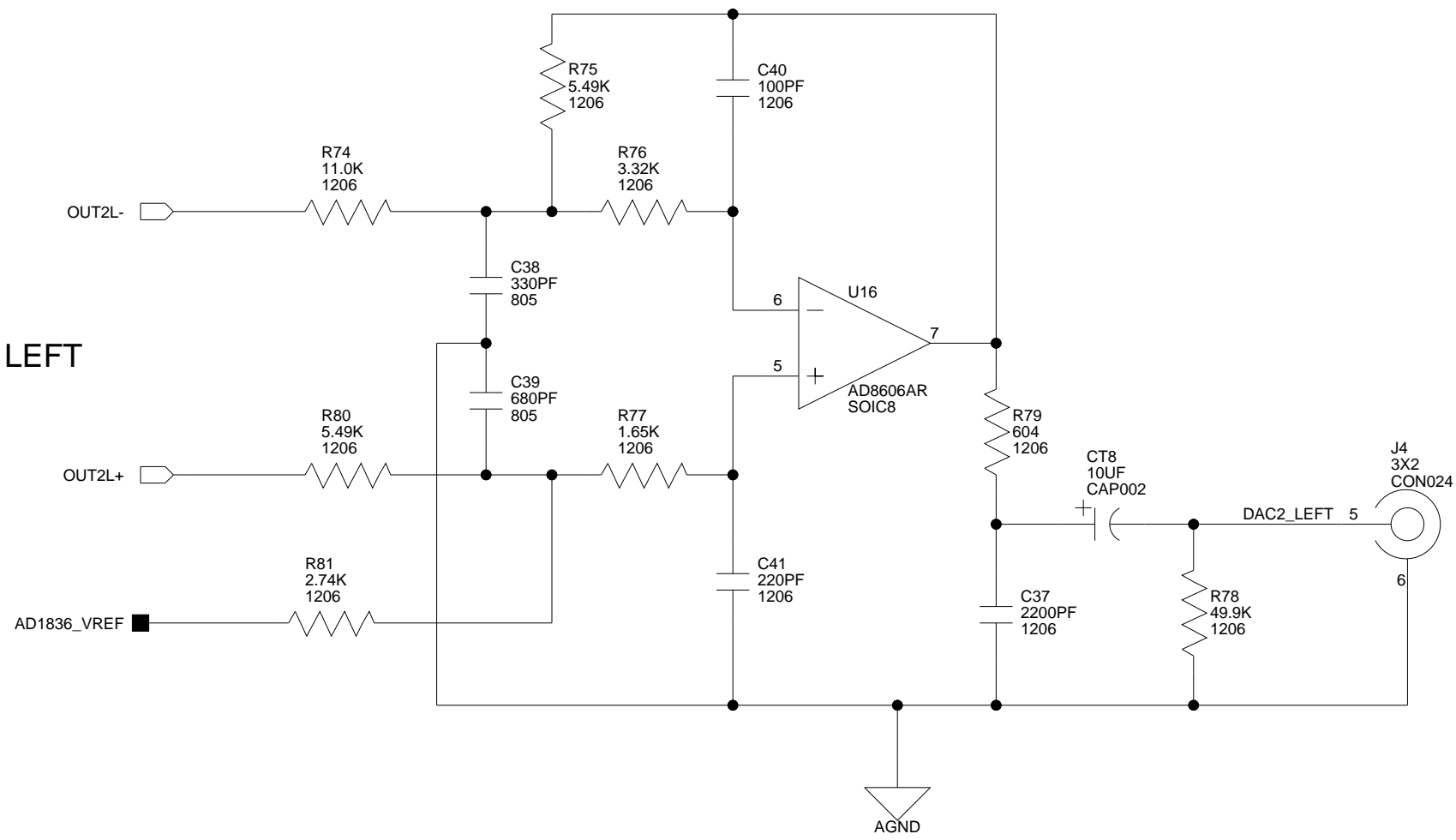
DAC2 RIGHT



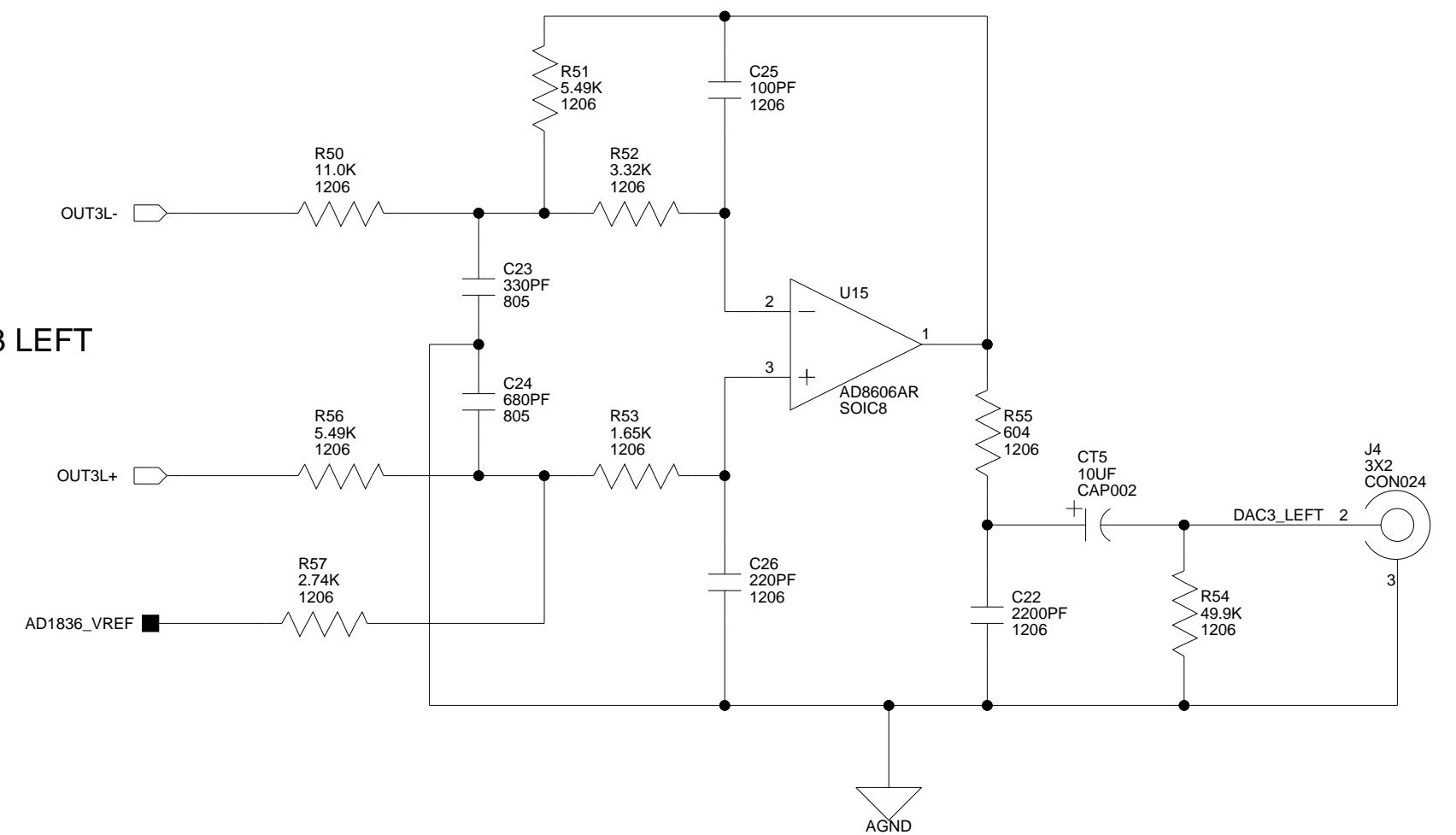
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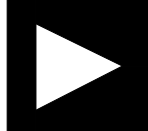
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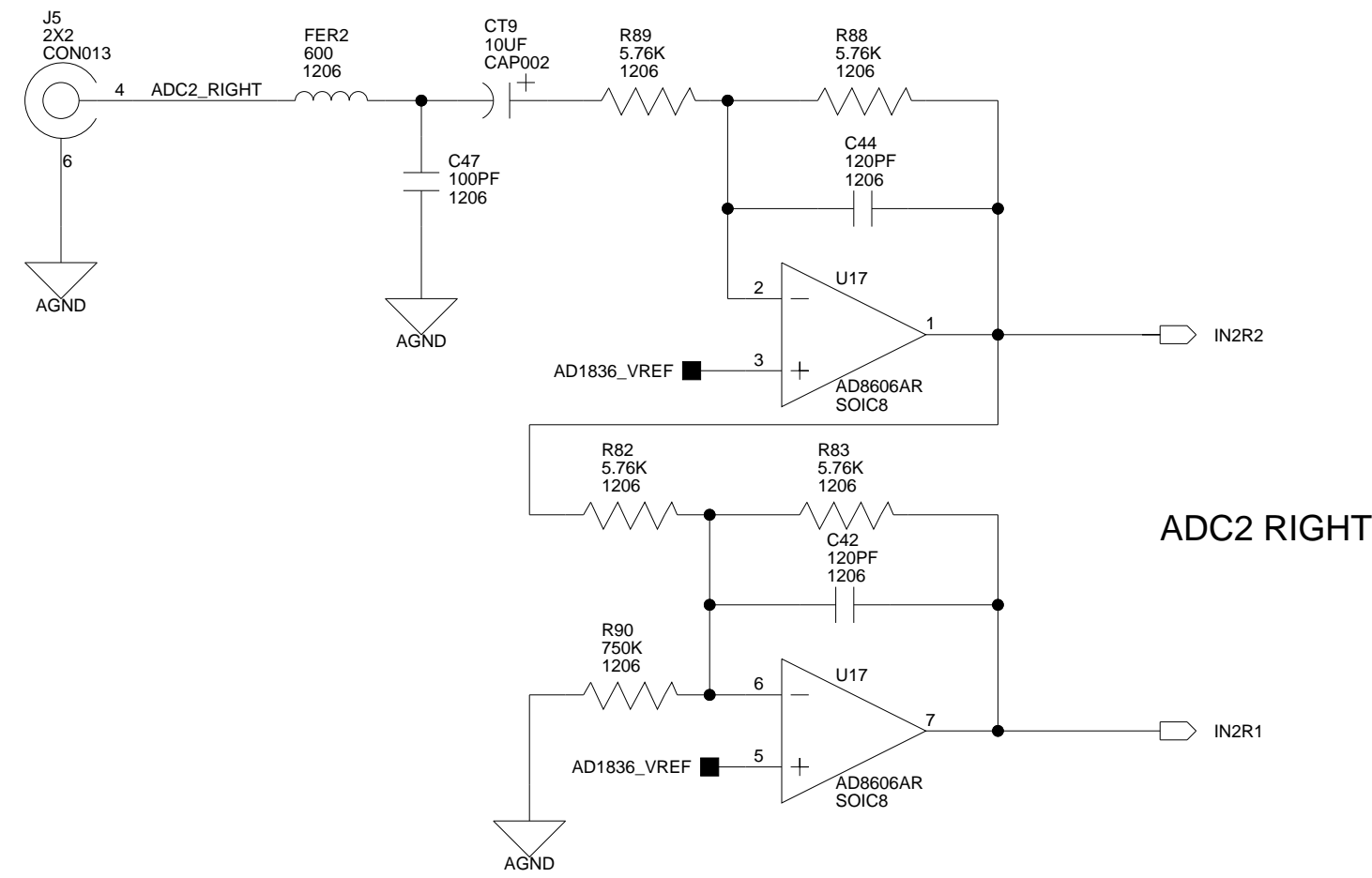
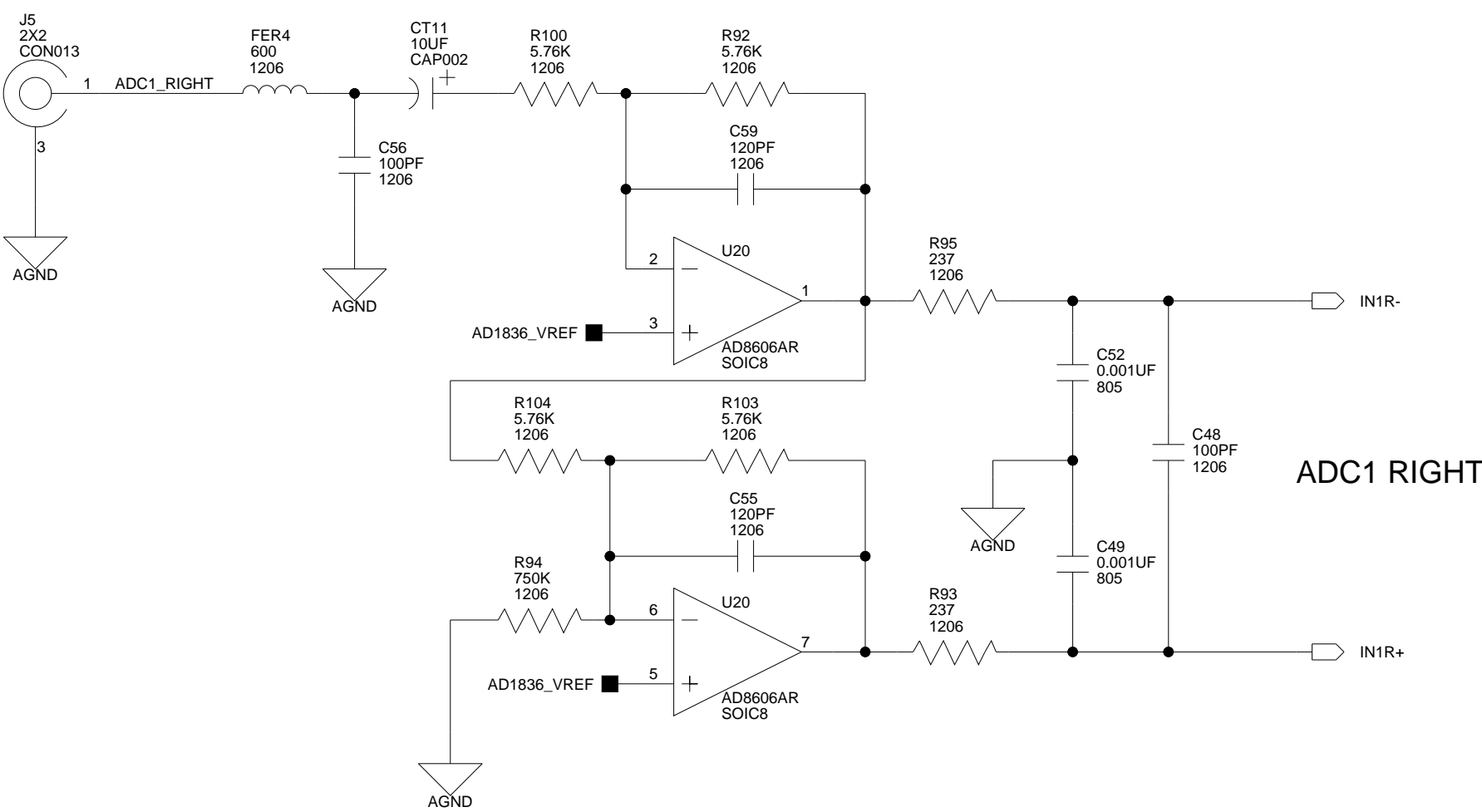
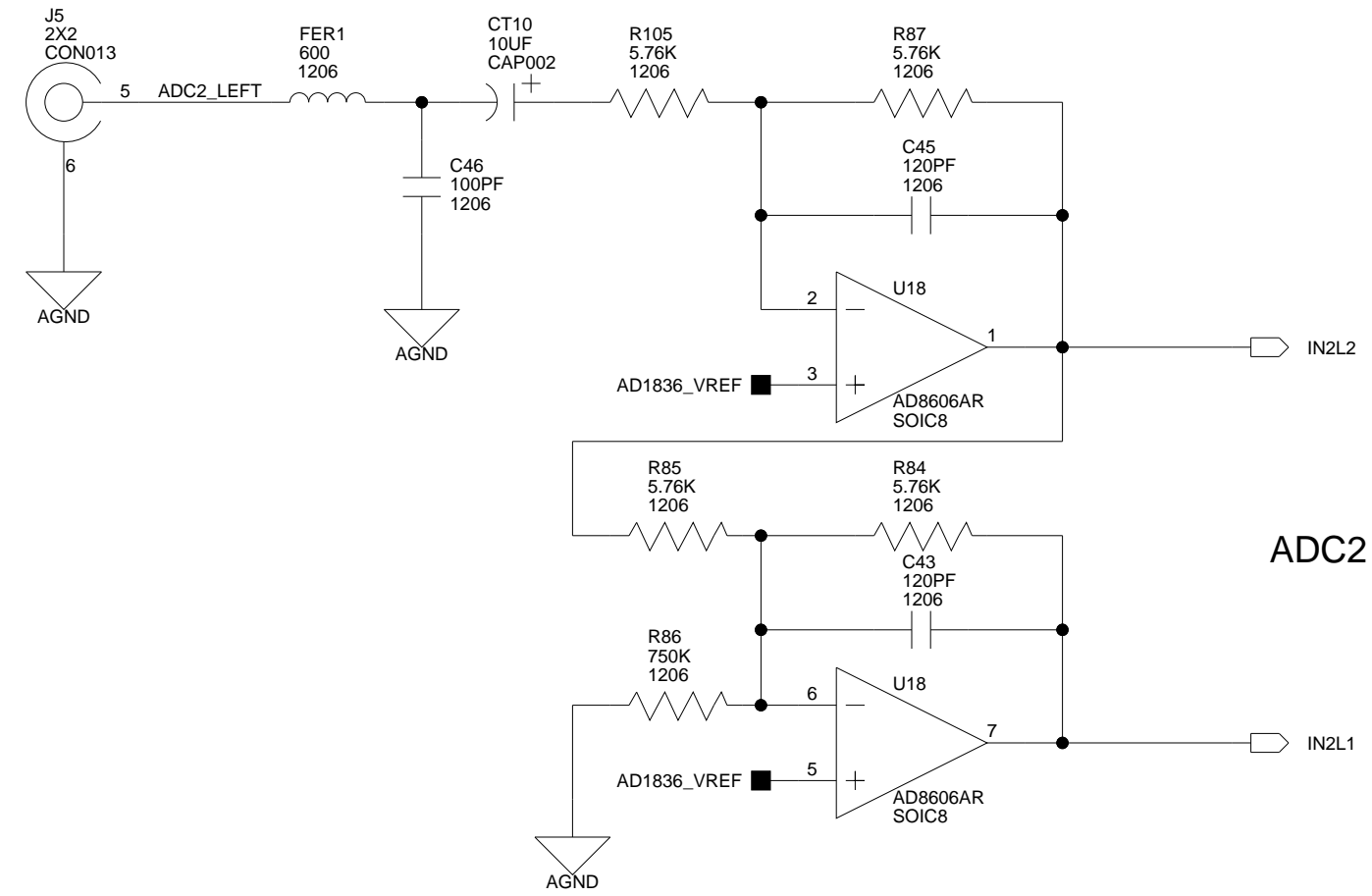
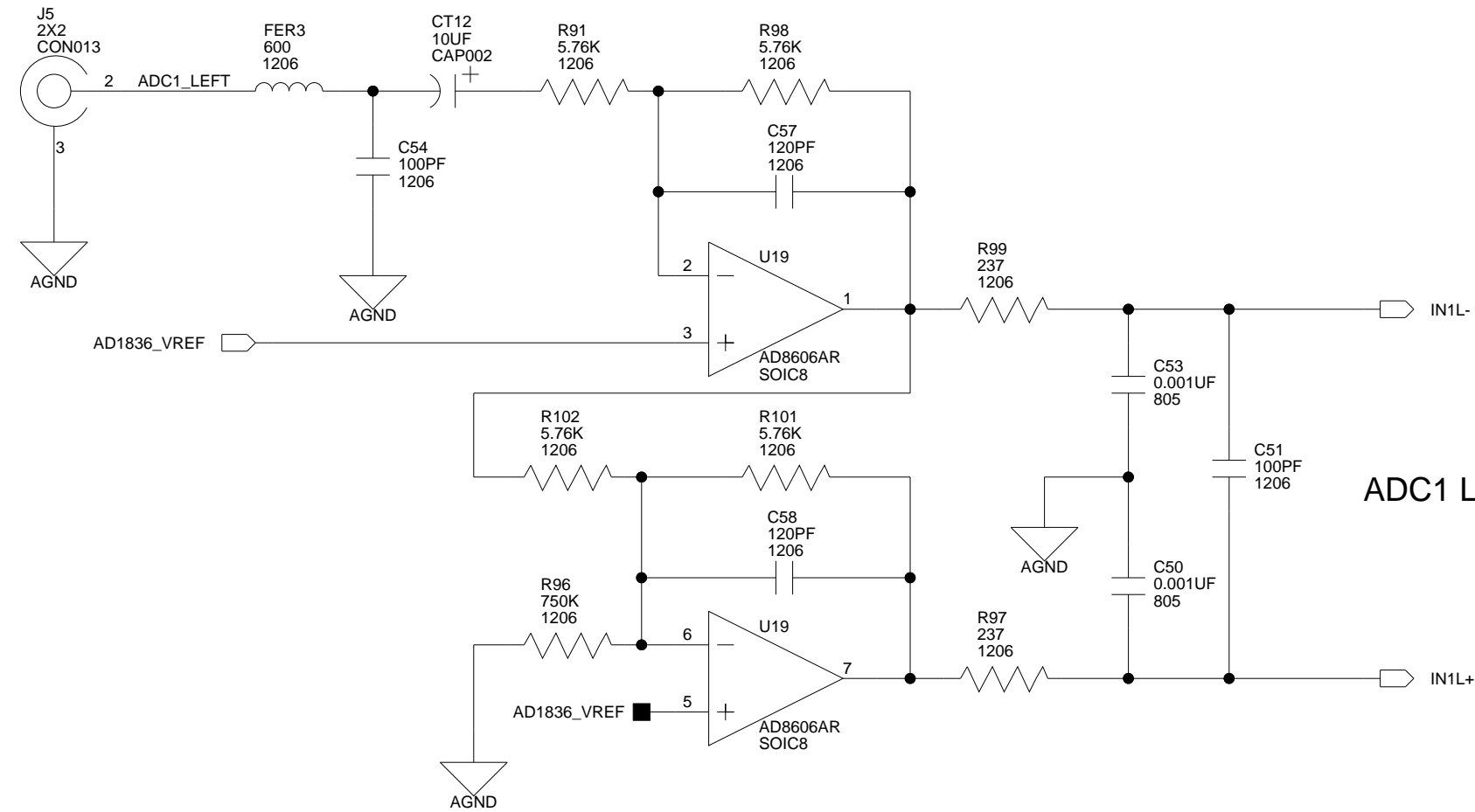


DAC3 LEFT



DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF533 EZ-KIT LITE - AUDIO OUT	
Approvals Drawn Checked Engineering		Date 12-21-2004_15:12	
Size C		Board No. A0167-2001	
Date 12-21-2004_15:12		Rev 1.6C	
Sheet 5		of 12	



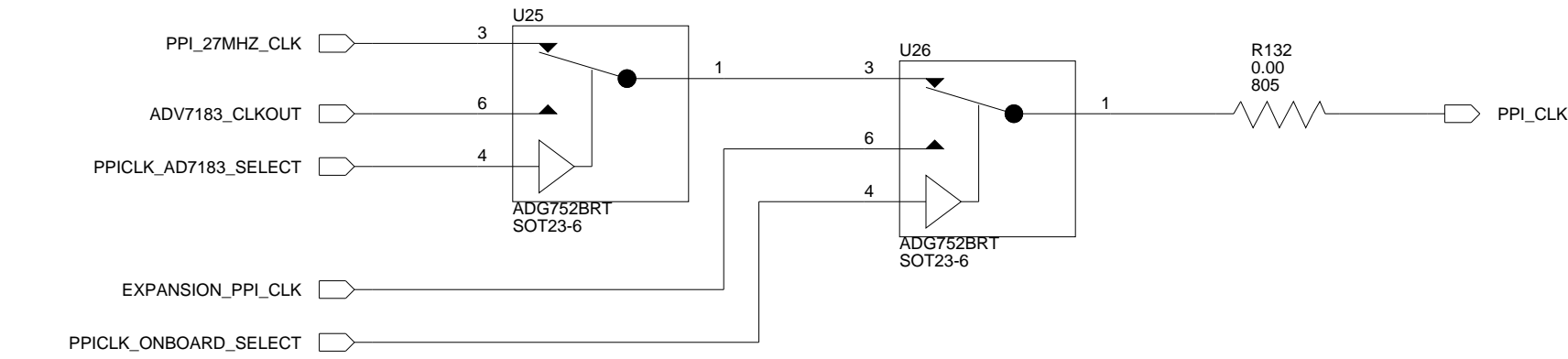
DNP = Do Not Populate

 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF533 EZ-KIT LITE - AUDIO IN	
Size C	Board No. A0167-2001	Rev 1.6C	
Date 12-21-2004_15:12	Sheet 6 of 12		

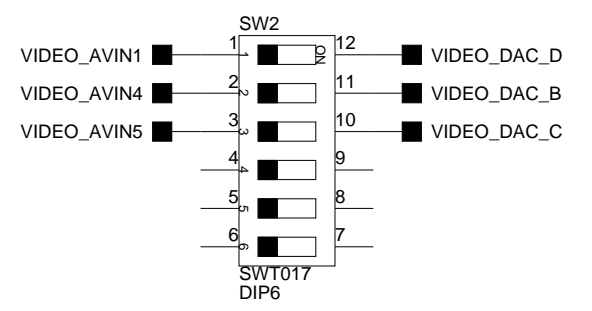
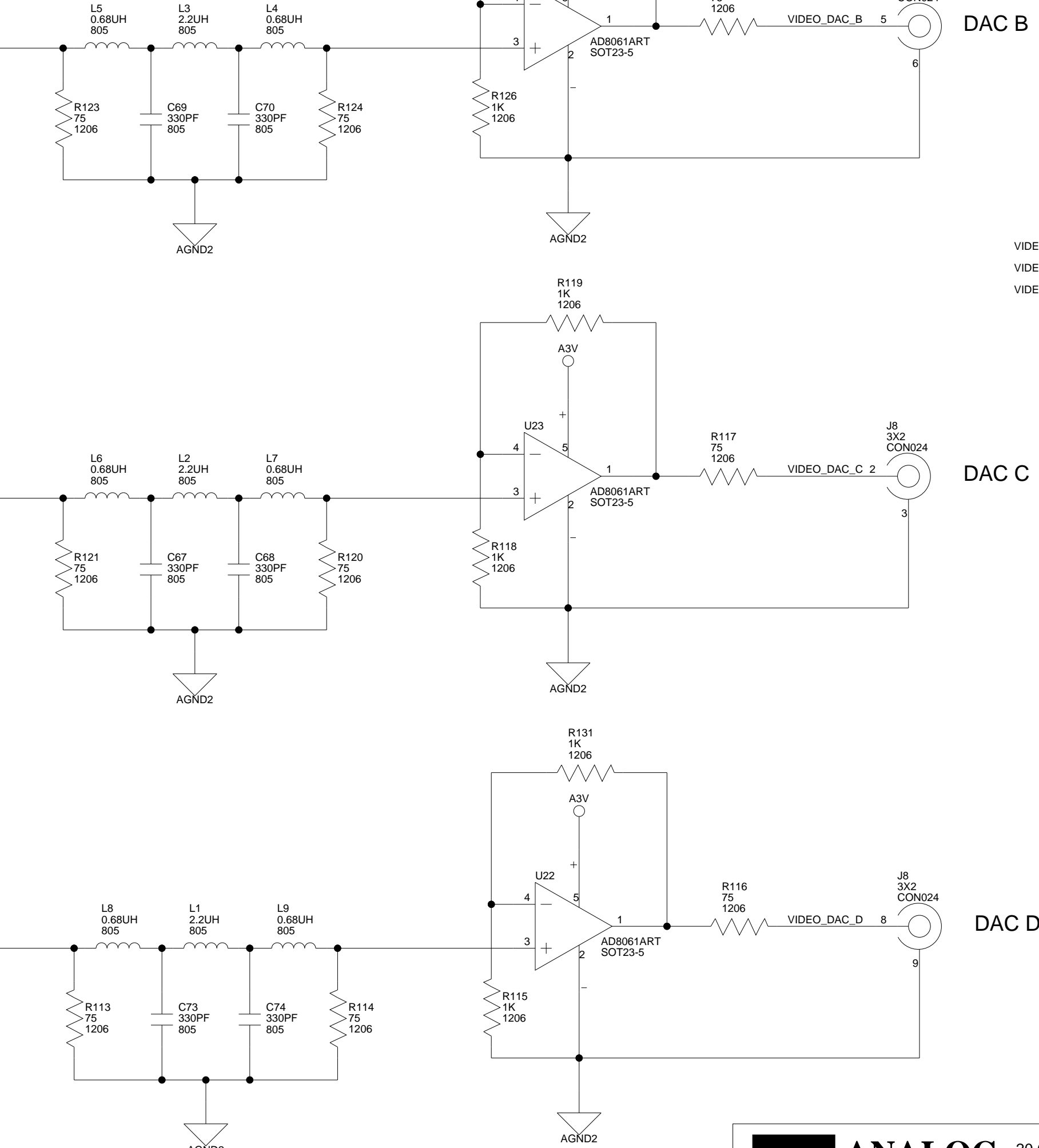
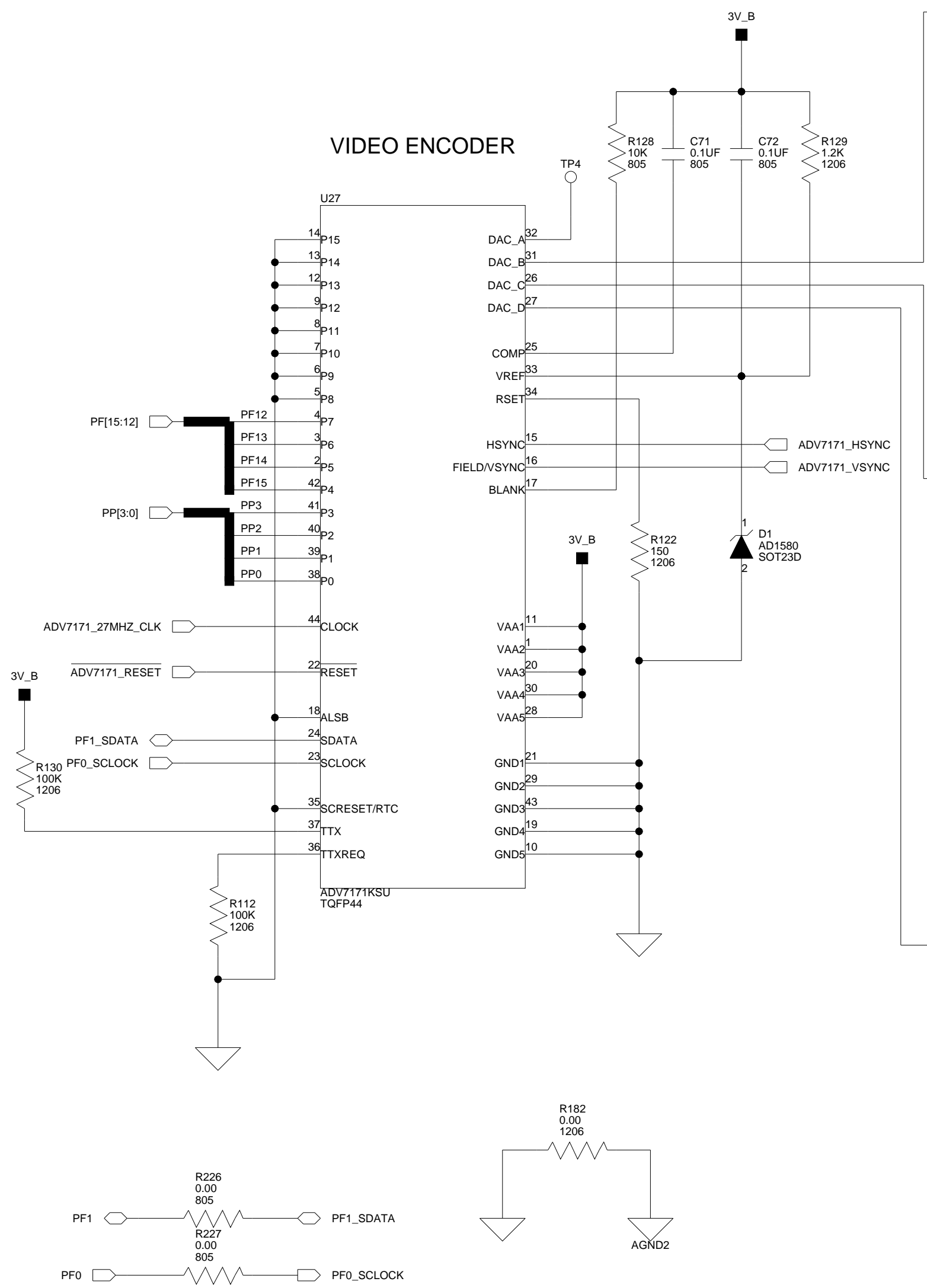
Approvals	Date
Drawn	
Checked	
Engineering	

PPICLK_ONBOARD_SELECT	PPICLK_AD7183_SELECT	PPCLK
0	0	PPL_27MHZ_CLK (DEFAULT)
0	1	ADV7183_CLKOUT
1	X	EXPANSION_CLK

	DAC B	DAC C	DAC D
Composite Video	CVSB		CVSB
Component Video	B	R	G
Differential Component Video	U	V	Y
S Video		C	Y



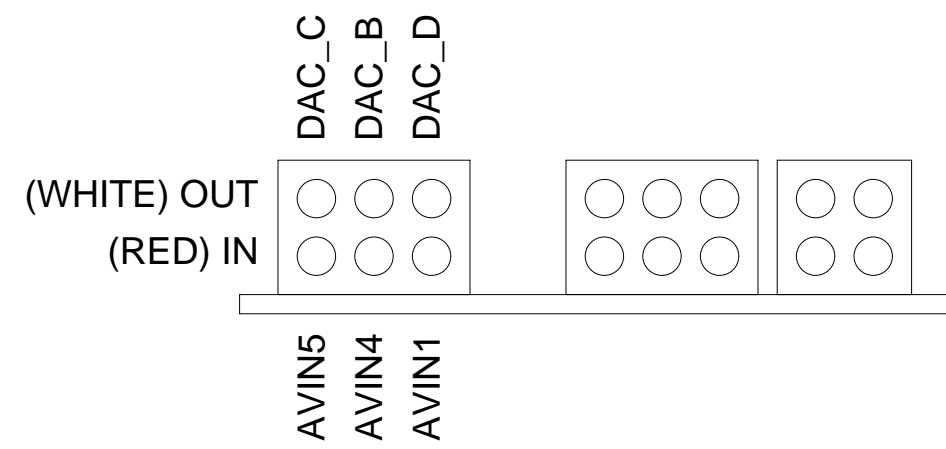
VIDEO ENCODER



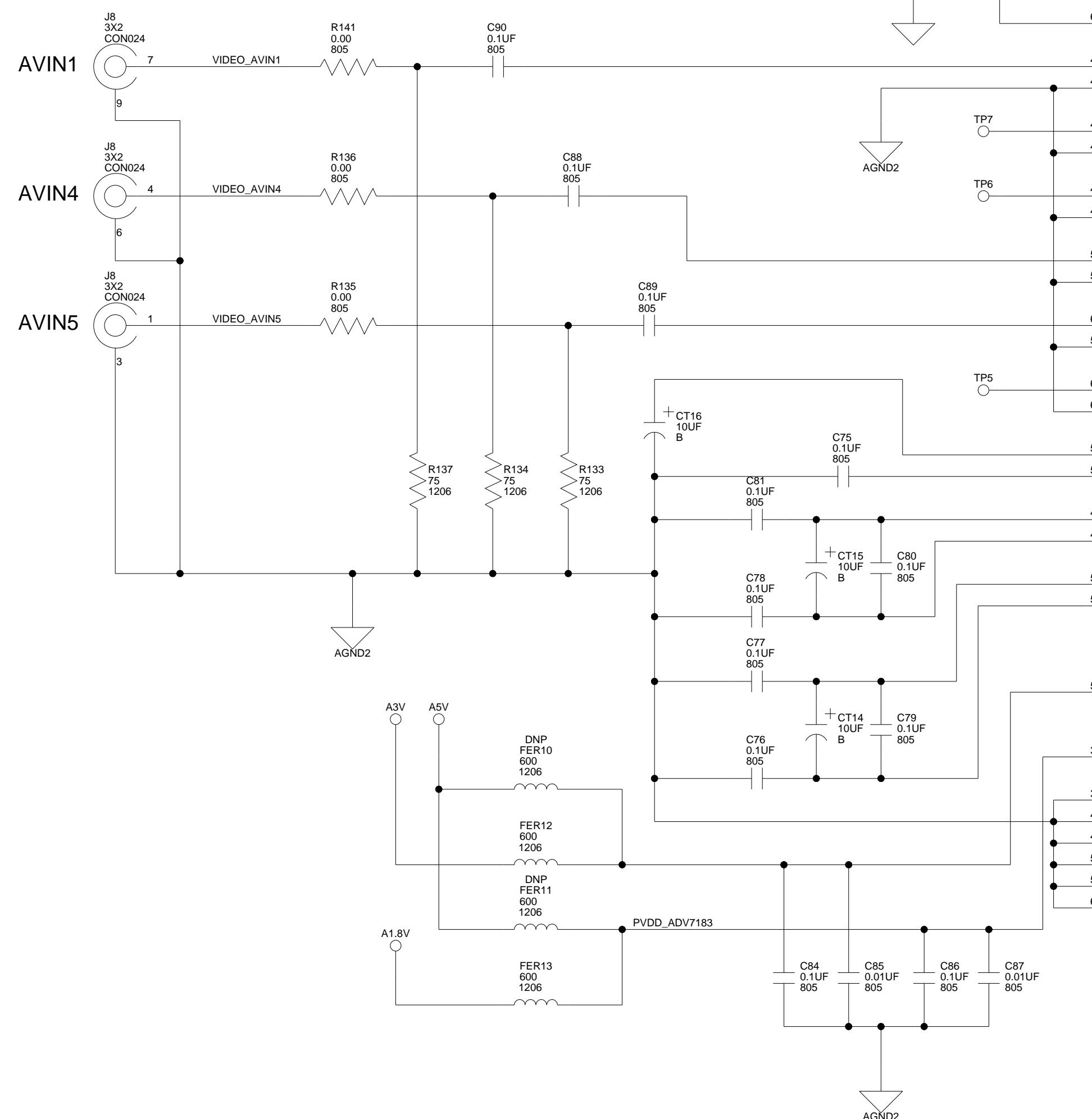
DNP = Do Not Populate

		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF533 EZ-KIT LITE - VIDEO OUT	
Size C		Board No. A0167-2001	
Date 12-21-2004_15:12		Rev 1.6C	
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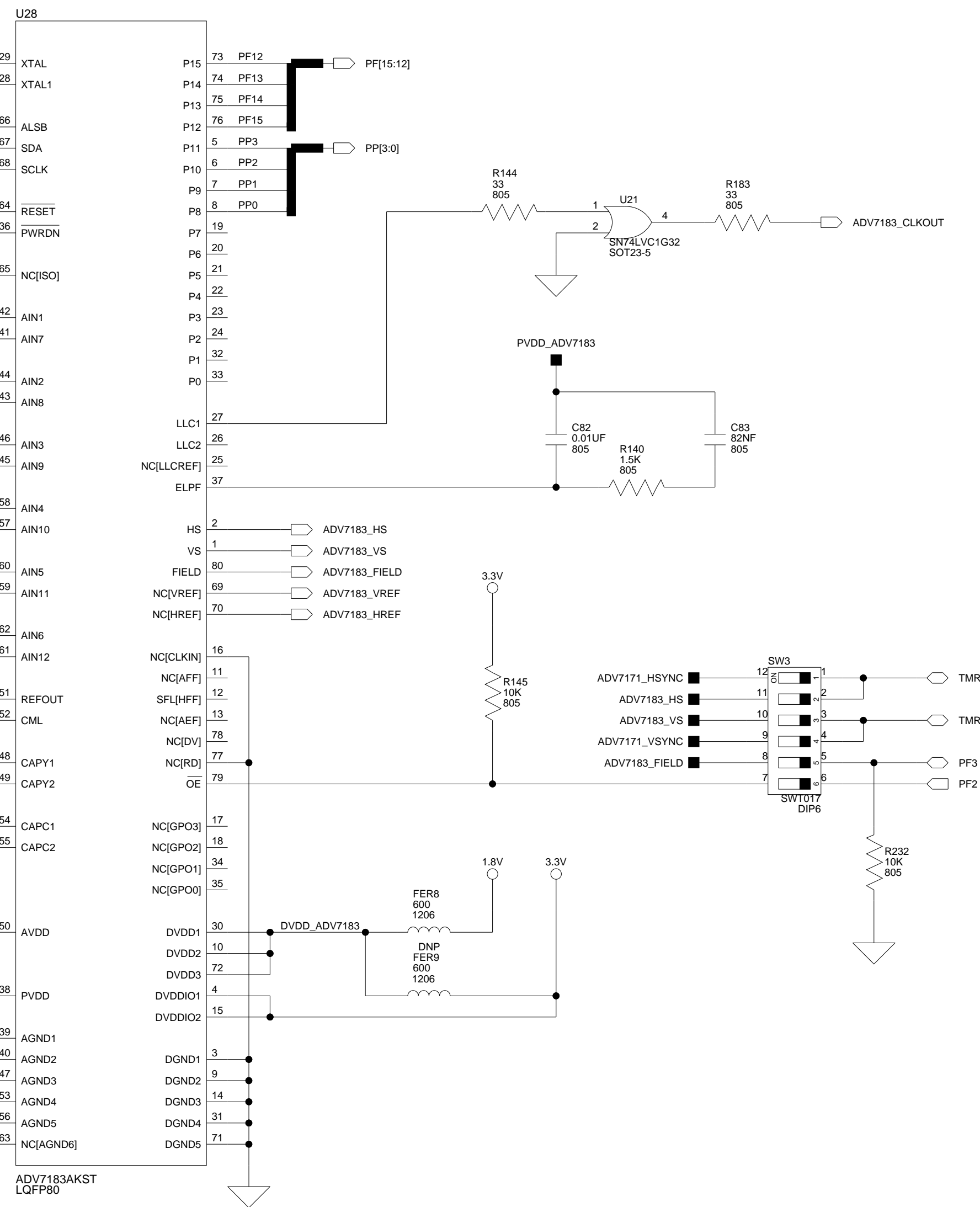
Approvals	Date
Drawn	
Checked	
Engineering	



	AVIN1	AVIN4	AVIN5
Composite Video	CVBS	CVBS	CVBS
Differential Component Video	Y	U	V
S Video	Y	C	



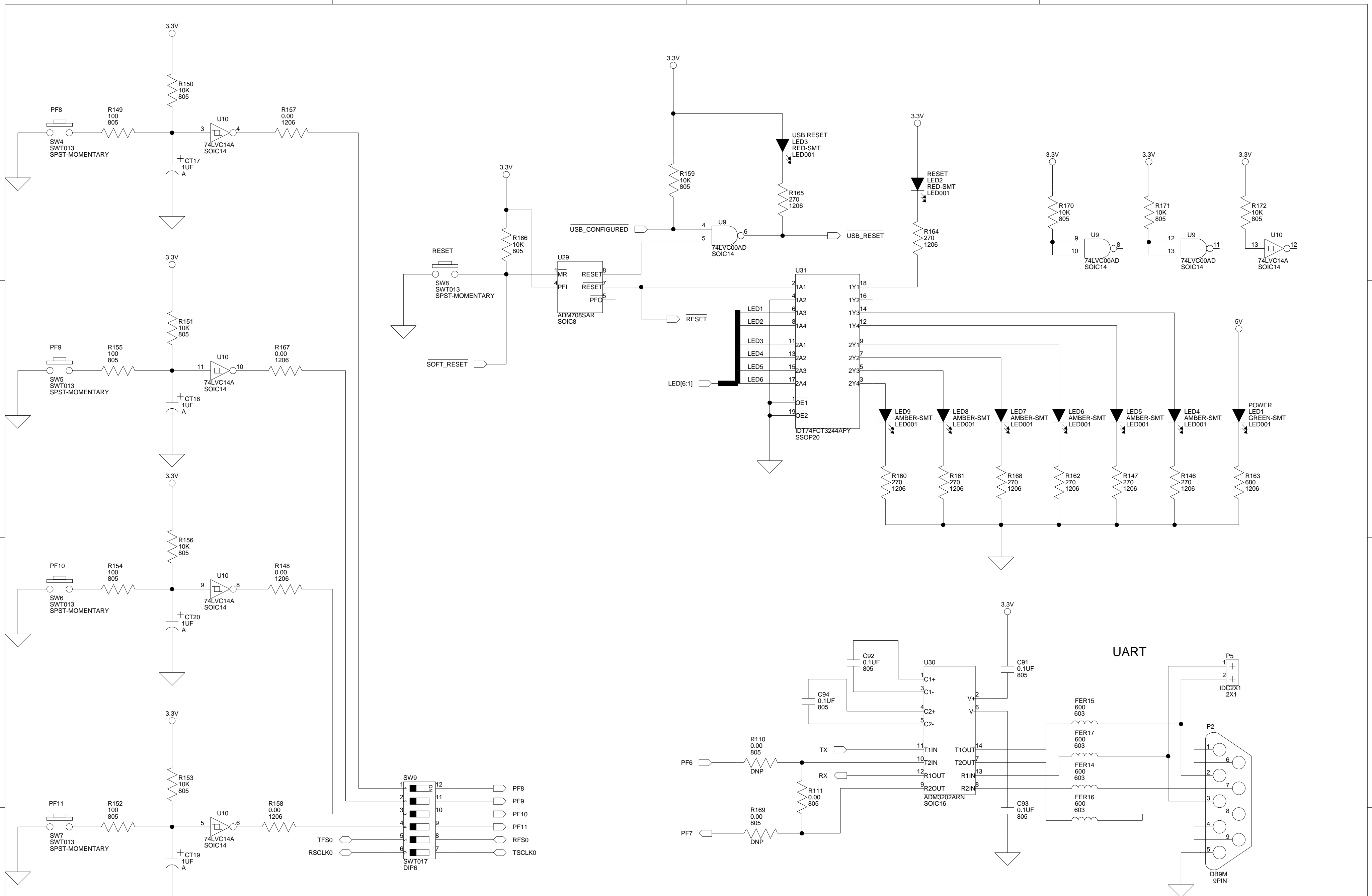
VIDEO DECODER



DNP = Do Not Populate

20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Approvals	Date	Title ADSP-BF533 EZ-KIT LITE - VIDEO IN		
Drawn		Size C	Board No. A0167-2001	Rev 1.6C
Checked		Date 12-21-2004_15:12	Sheet 8 of	12
Engineering				



SW8 PB Enable Switch

Position	Function
1-4	Connects the push buttons to the Programmable Flags of the DSP Useful if using the PFs for another purpose.
5,6	Connects SPORT0 frame sync and clock together external to the DSP Required when AD1836 is in I2S mode

DNP = Do Not Populate

ANALOG DEVICES

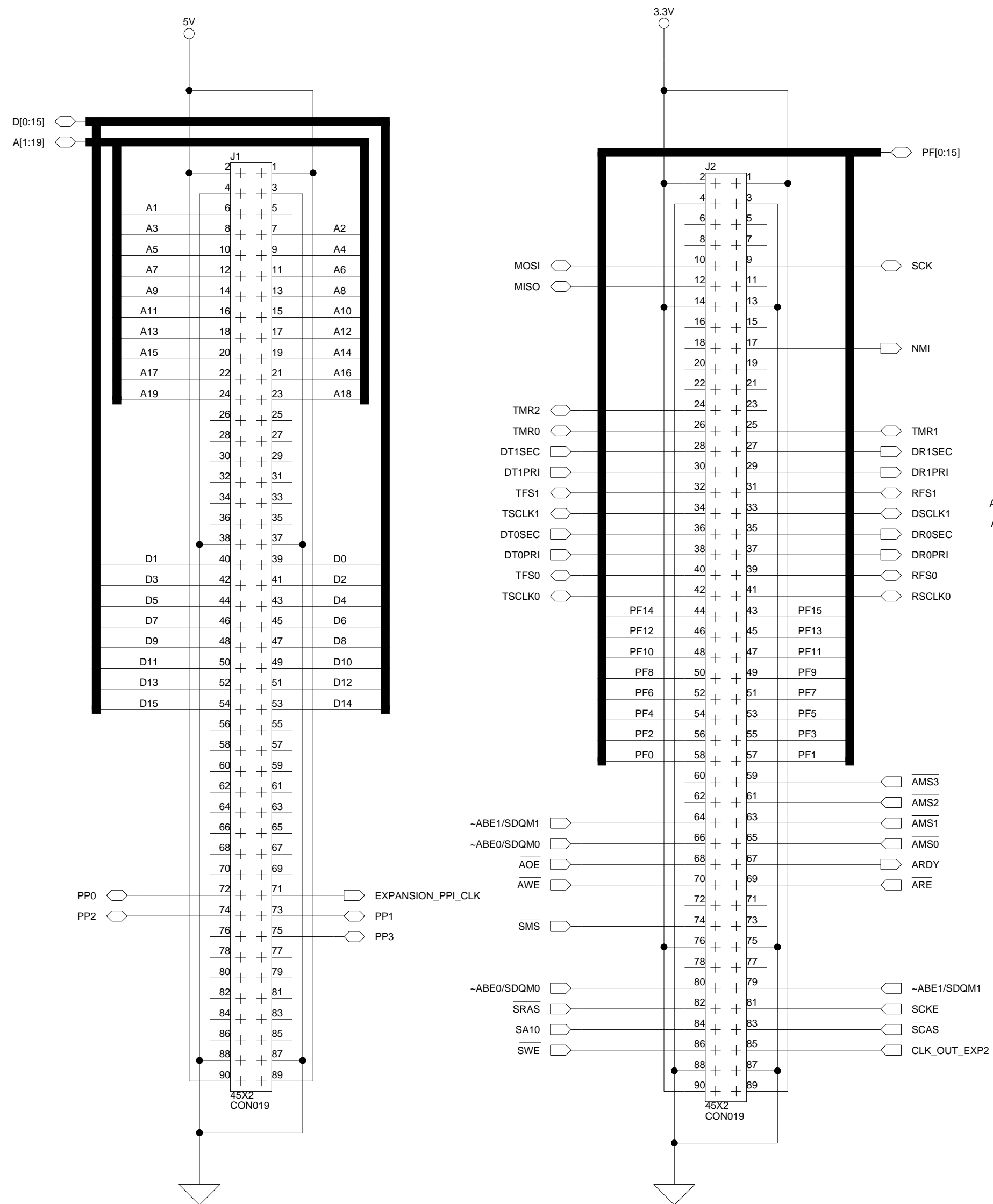
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title ADSP-BF533 EZ-KIT IO/RESET/UART

Size C	Board No. A0167-2001	Rev 1.6C
Date 12-21-2004_15:12	Sheet 9 of 12	

Approvals	Date
Drawn	
Checked	
Engineering	

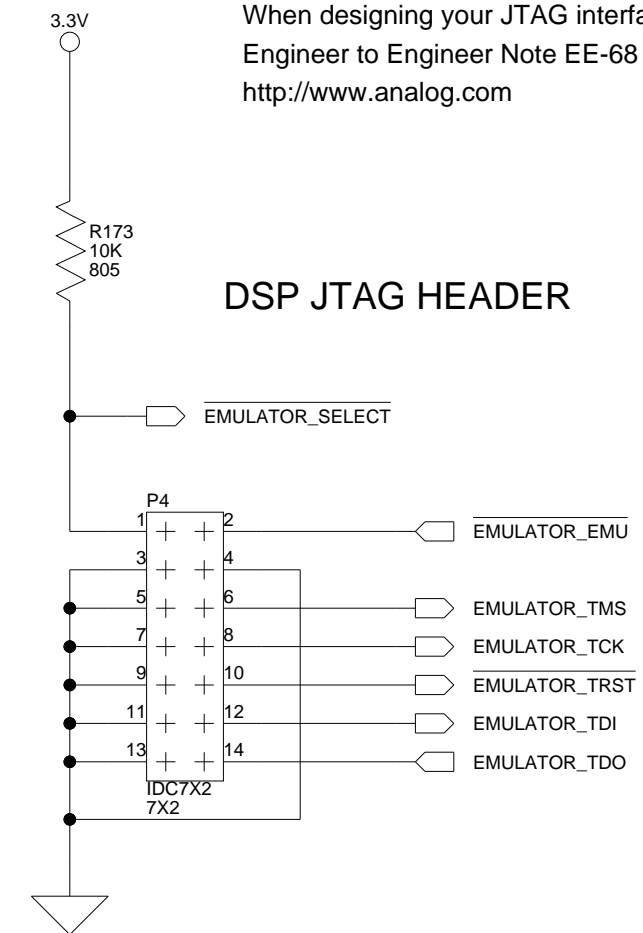
EXPANSION INTERFACE (TYPE B)



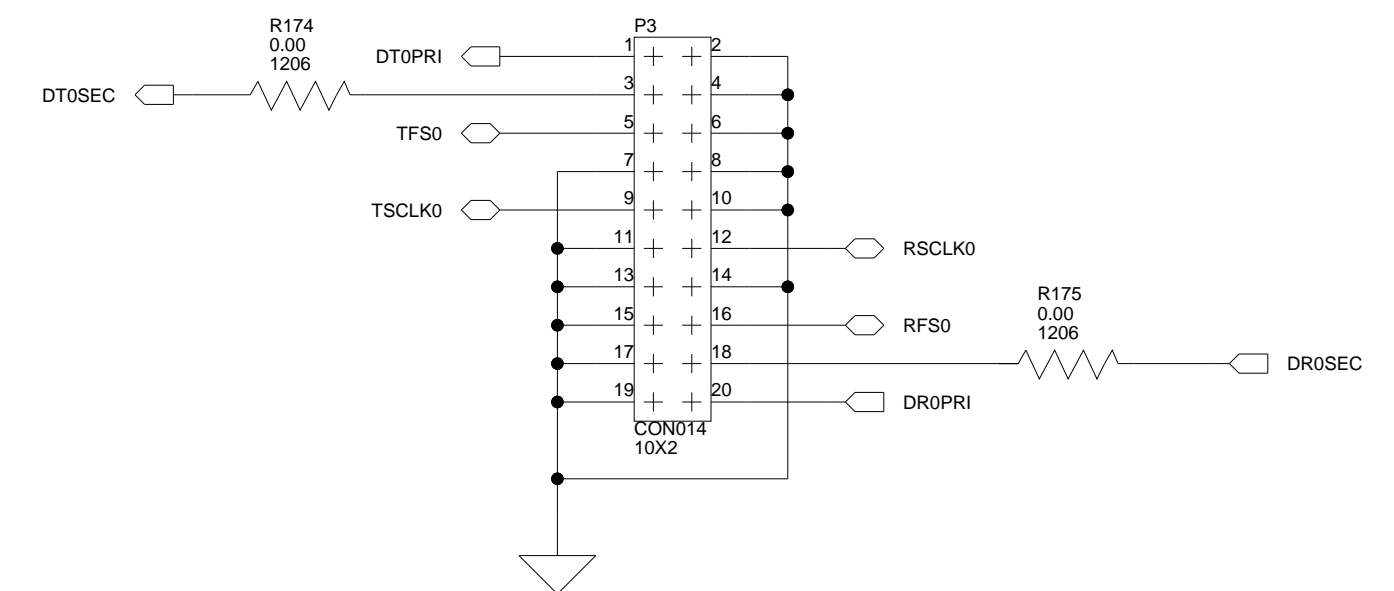
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at <http://www.analog.com>

DSP JTAG HEADER



SPORT0



DNP = Do Not Populate

		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-BF533 EZ-KIT LITE - CONNECTOR	
Size C	Board No. A0167-2001	Rev 1.6C	
Date 12-21-2004_15:11	Sheet 10 of 12		

Approvals	Date
Drawn	
Checked	
Engineering	

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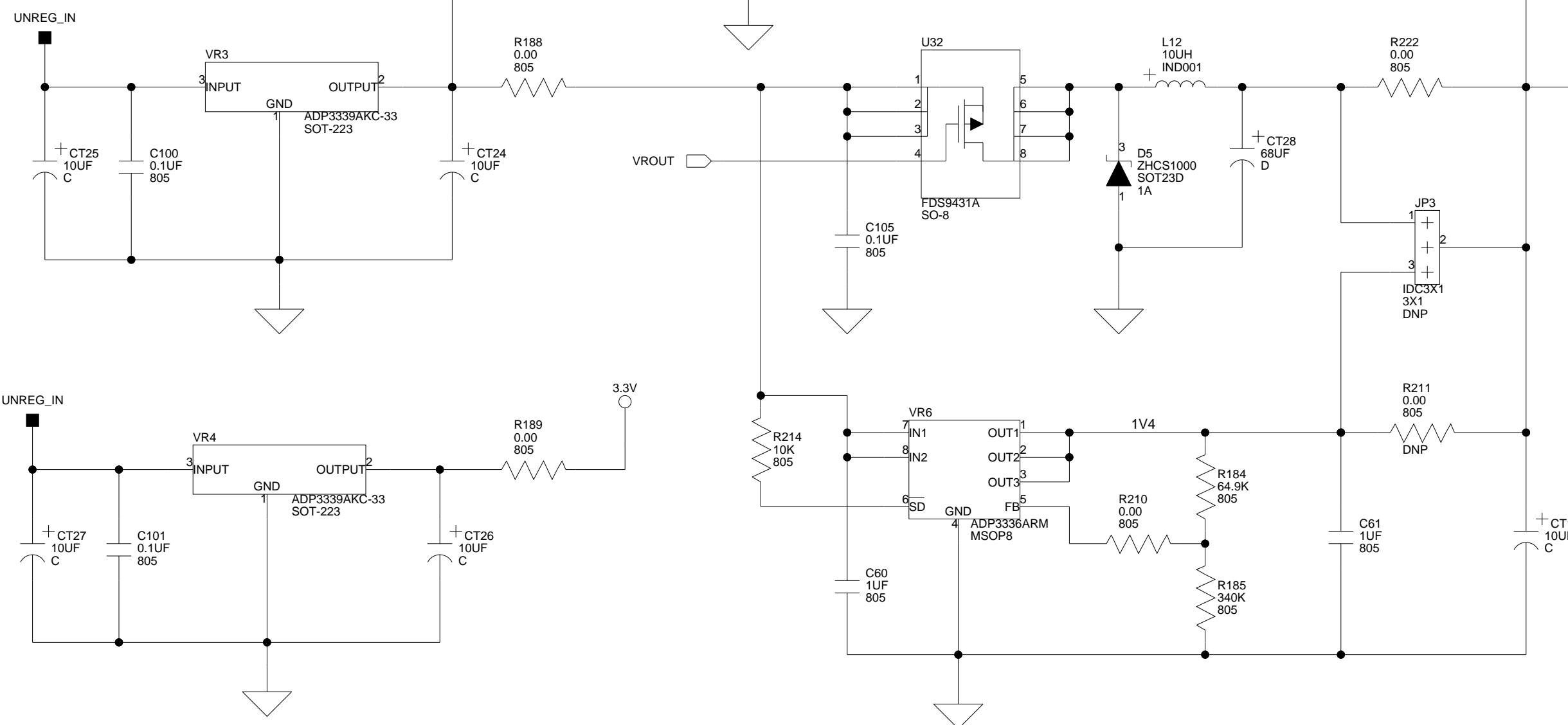
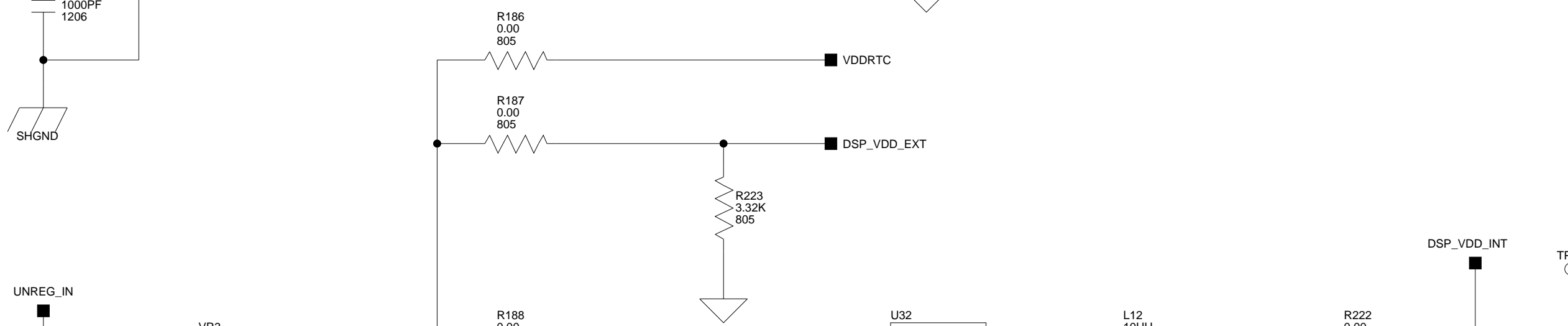
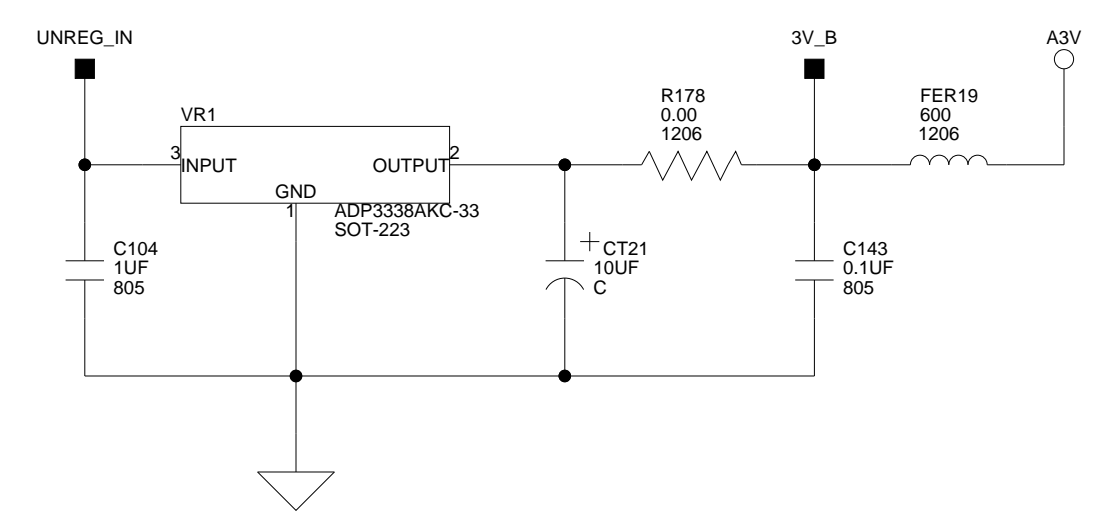
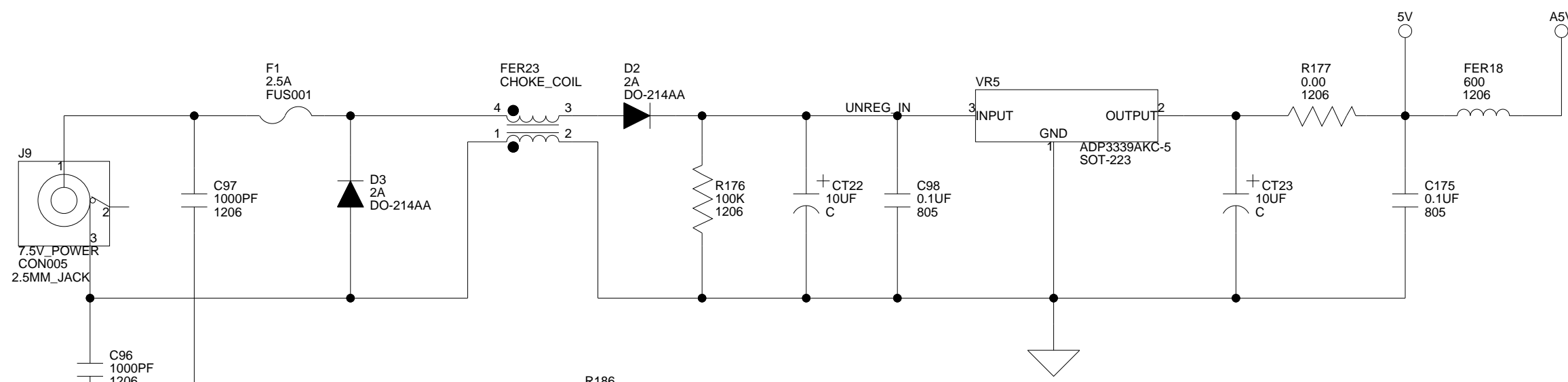
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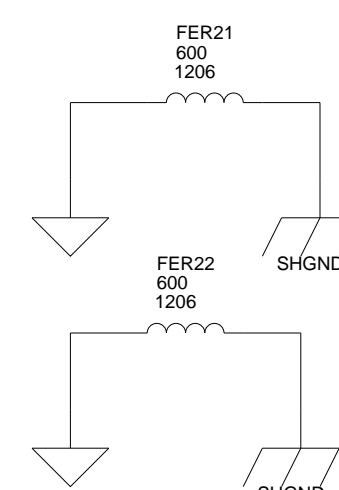
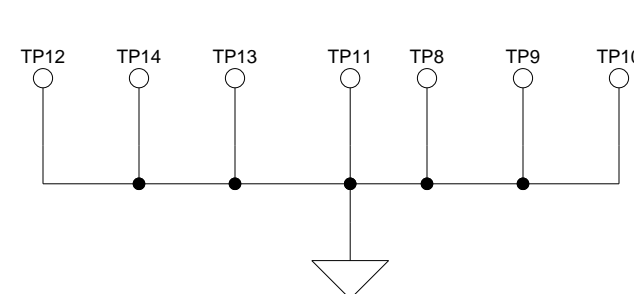
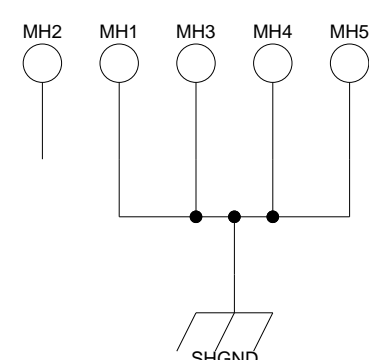
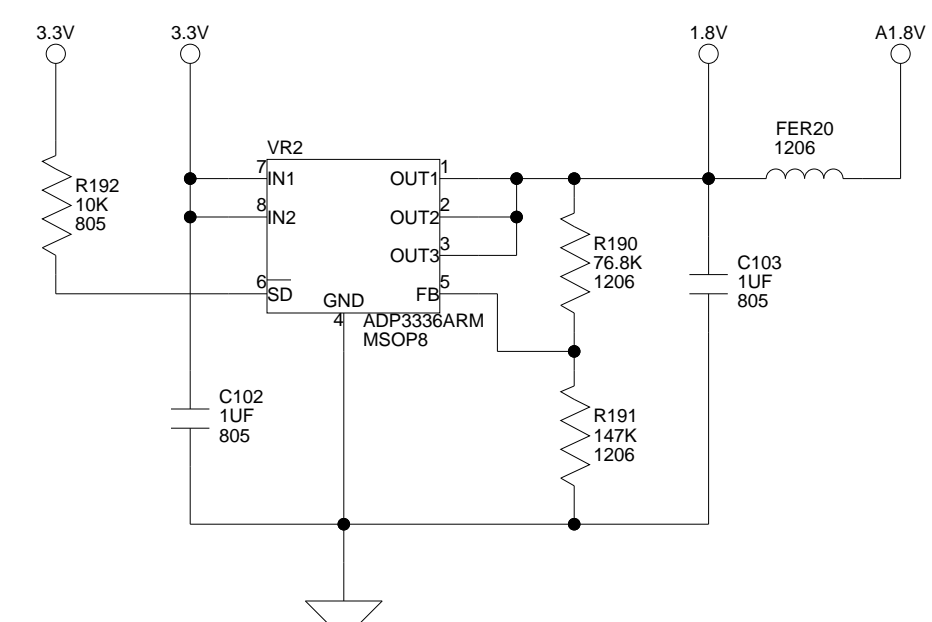
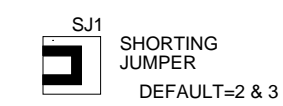
4



SW10: Core Voltage Source Select
DEFAULT: Not Populated

Position	Function
1 and 2	DSP_VDD_INT = DSP Internal Voltage Regulation
2 and 3	DSP_VDD_INT = 1.4V Fixed

Note: For boards without a 750MHz processor this jumper will not be populated and the DSP_VDD_INT will be hard-wired with R222 to use the processor internal regulator.



DNP = Do Not Populate

ANALOG DEVICES

20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Approvals		Date		Title	
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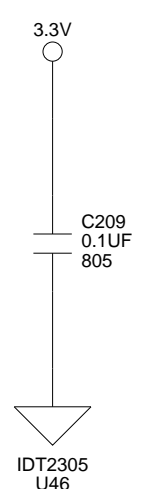
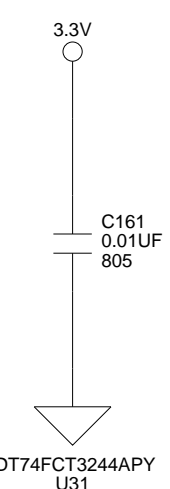
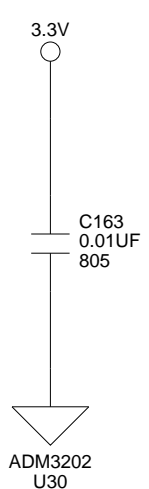
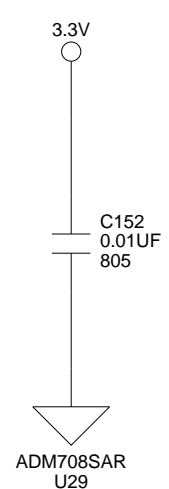
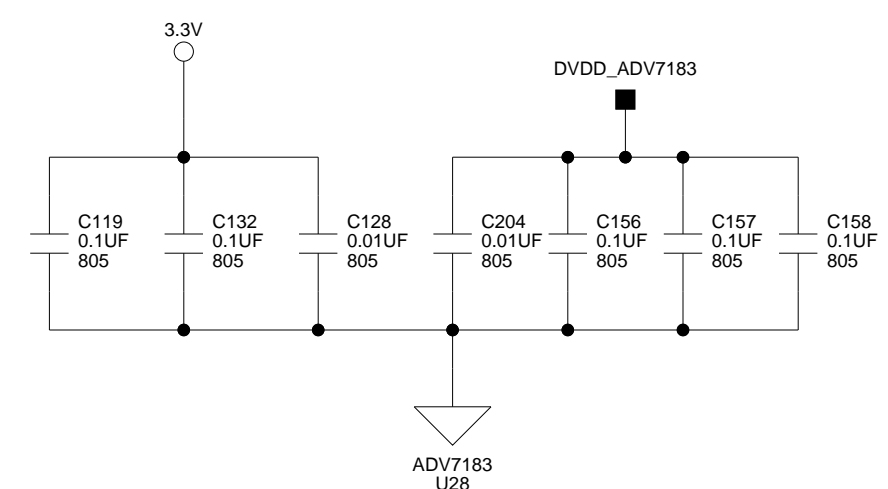
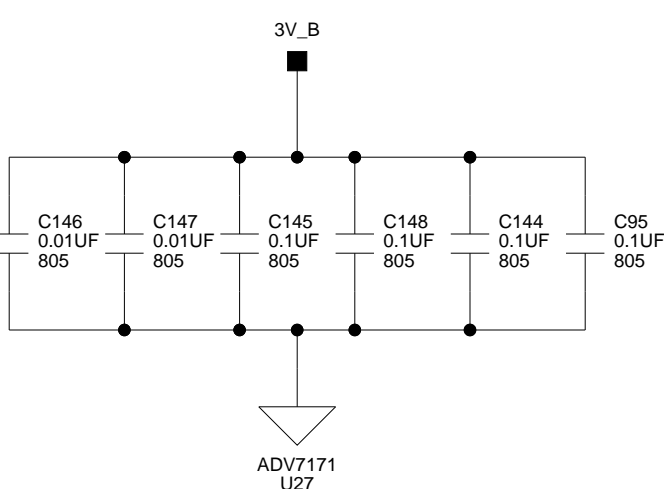
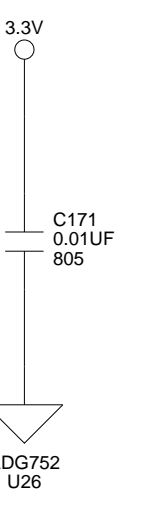
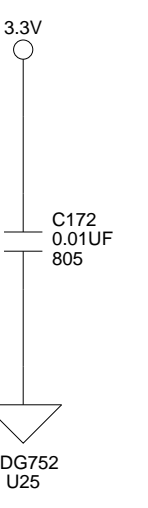
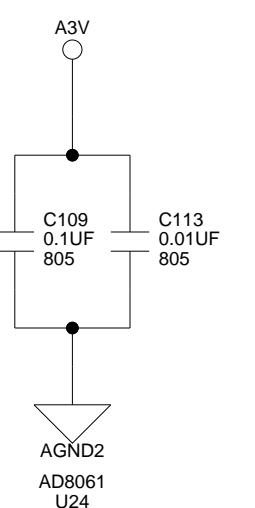
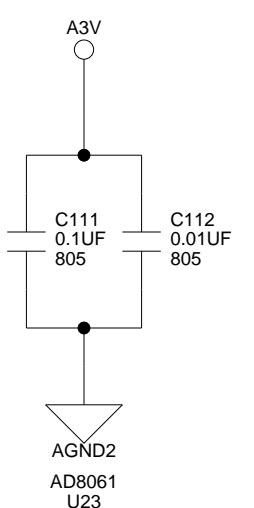
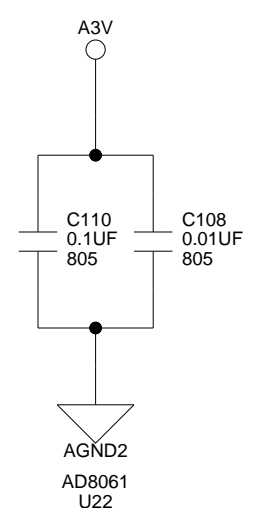
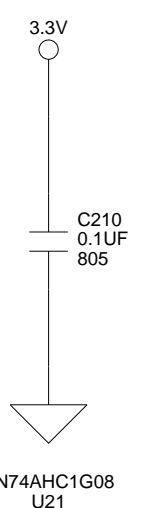
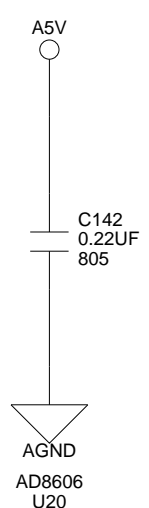
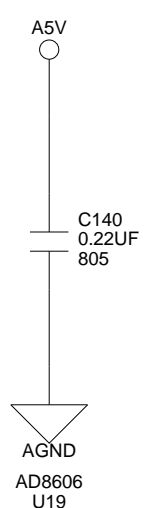
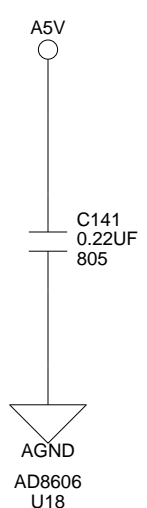
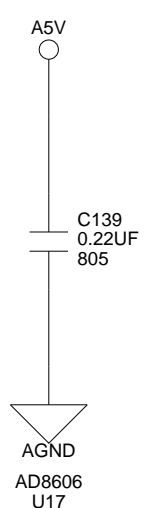
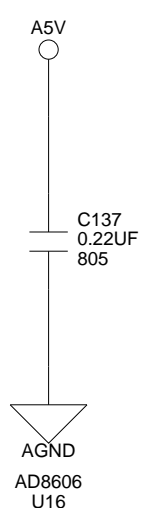
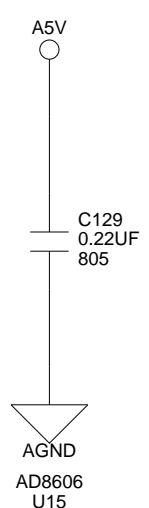
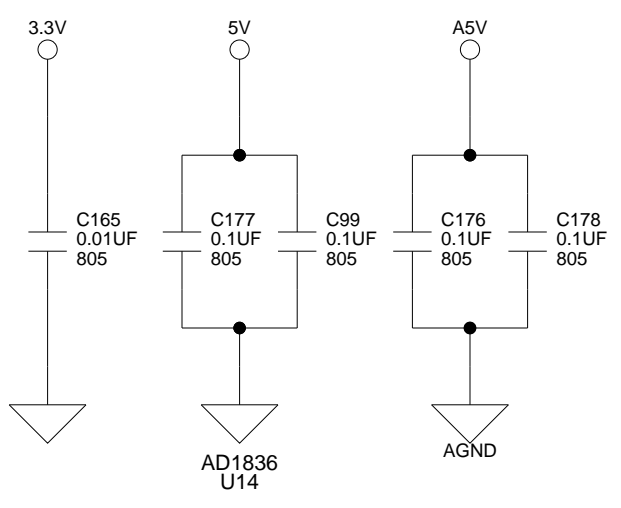
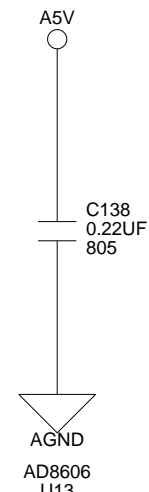
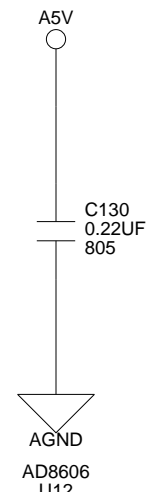
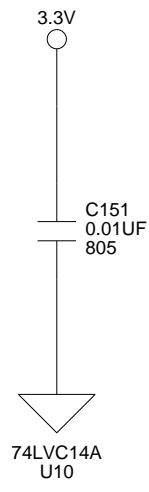
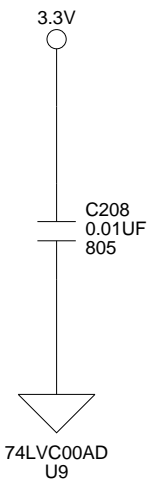
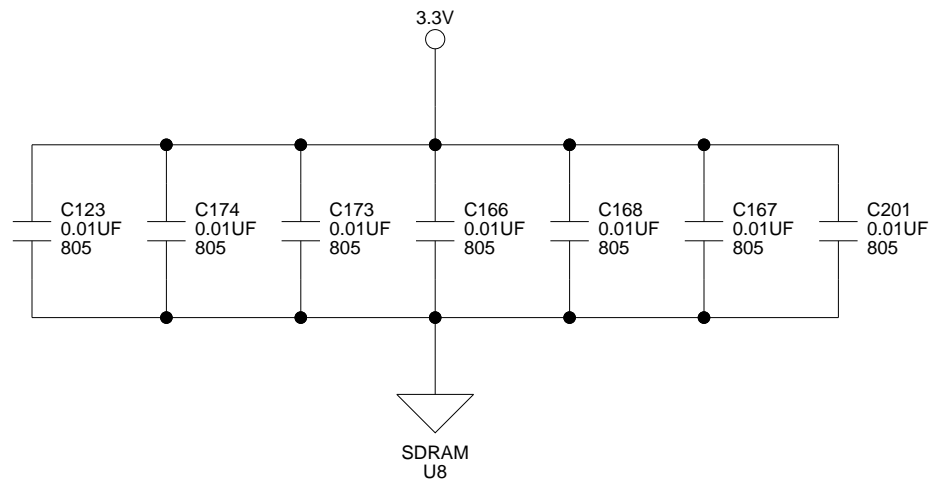
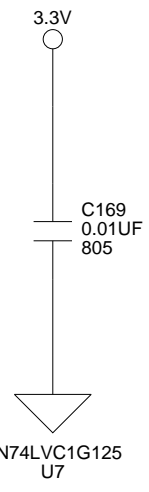
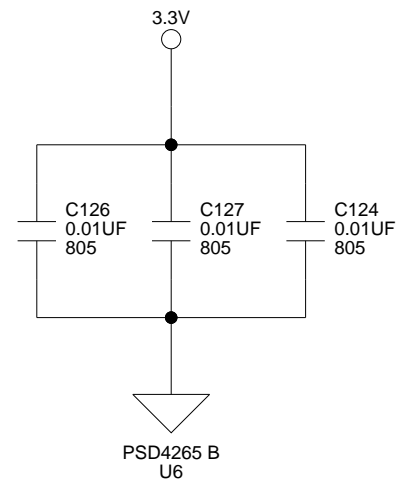
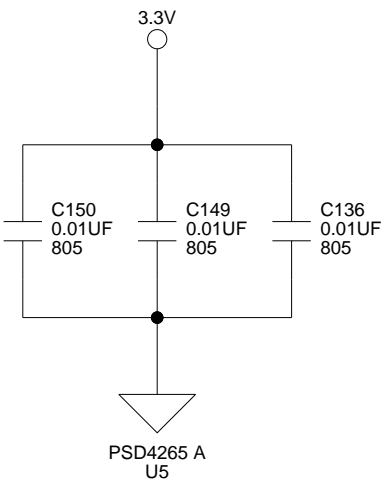
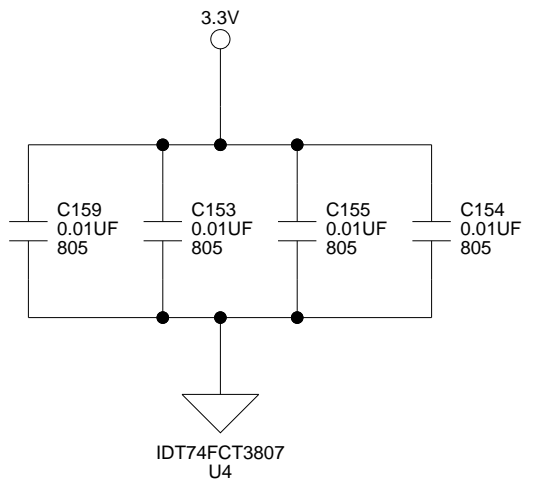
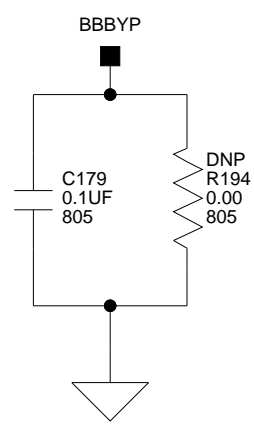
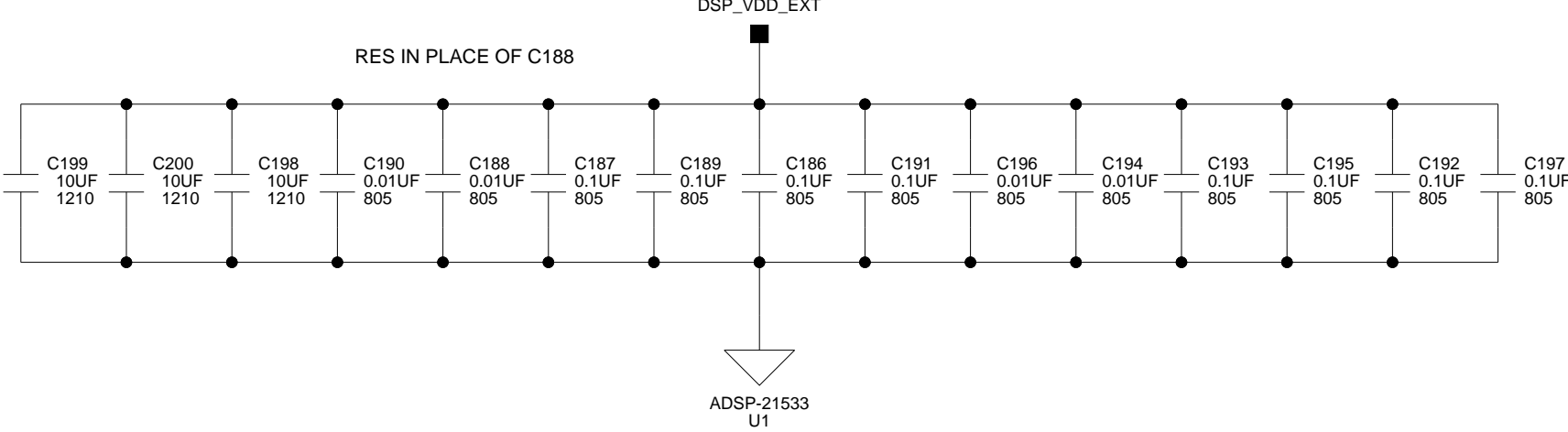
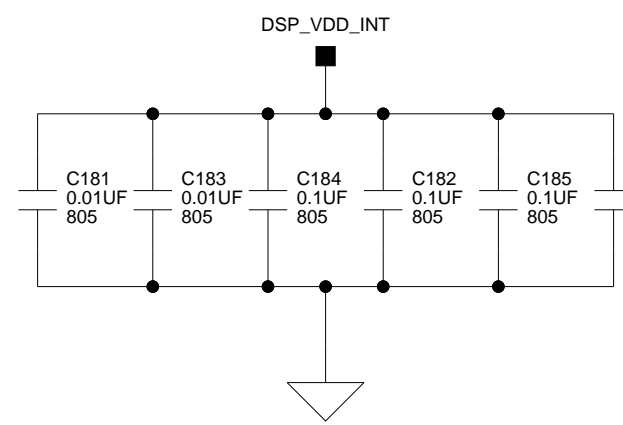
Title		ADSP-BF533 EZ-KIT LITE - POWER	
Size C		Board No.	
Date		Sheet	

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DNP = Do Not Populate

Approvals		Date		Title ADSP-BF533 EZ-KIT LITE - BYPASS CAPS	
Drawn				Size C	
Checked				Board No. A0167-2001	
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