Revision History					
Date	**ECO#**	**Description**	**Sheet**	**Initiater**	**Approval**
	0.1	Capture the full schematic	1 to 13	Actel	
	0.2			Actel	
	0.3			Actel	
	0.4			Actel	
	0.5			Actel	
	0.6			Actel	
	0.7			Actel	
	0.8			Actel	
	0.9			Actel	
	1.1			Actel	
	1.2			Actel	
	1.3			Actel	
	1.4			Actel	
	1.5			Actel	
	1.6			Actel	
	1.7			Actel	

AFS System Supervisor Board

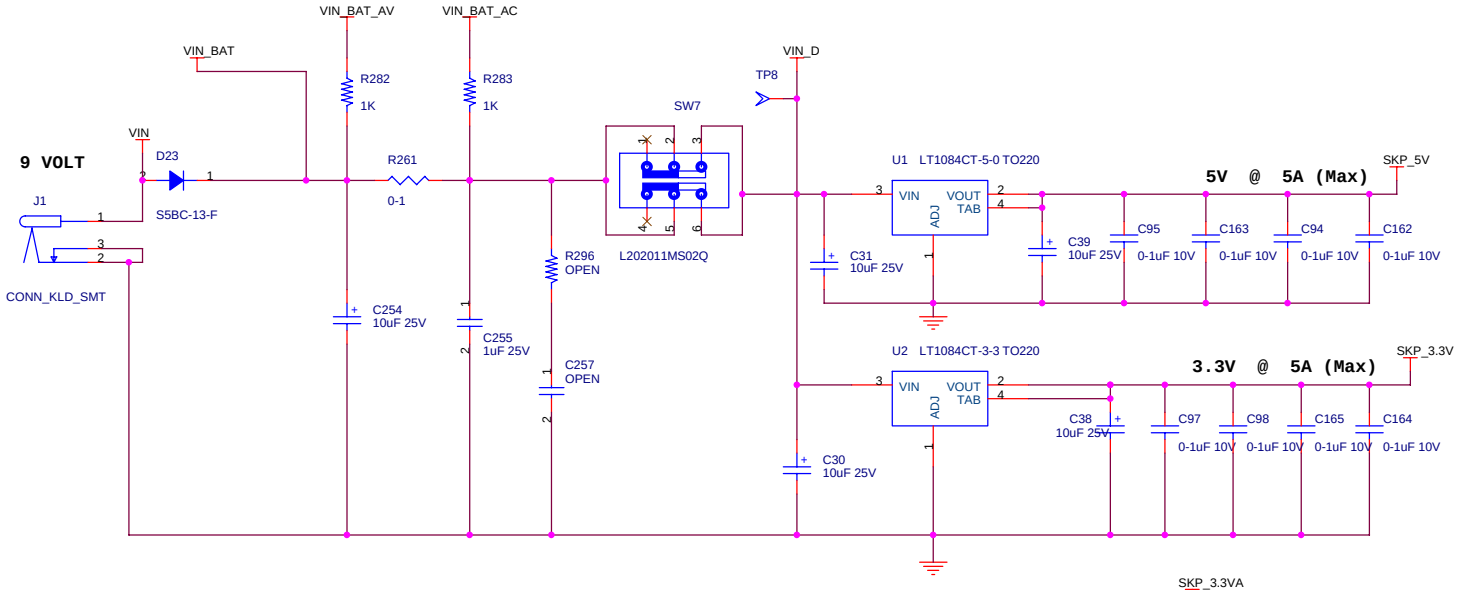
SCHEMATIC DIAGRAM NOTES
1.UNLESS STATED OTHERWISE:
  A.ALL RESISTOR ARE IN OHMS, 5% TOLERANCE.
  B.ALL CAPACITORS ARE IN MICROFARADS,10% TOLERANCE.

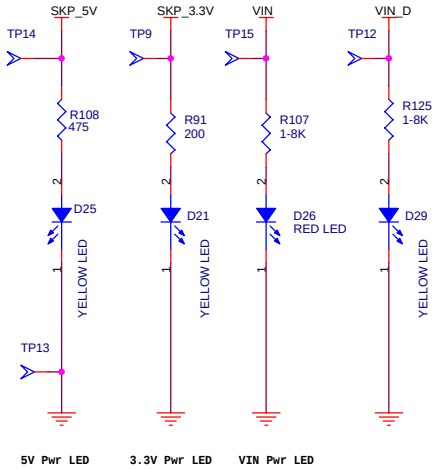
BOARD INFORMATION

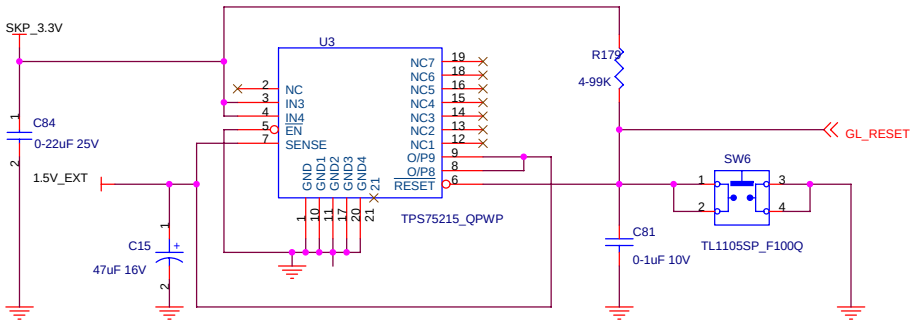
PCB FAB:,REV.0X PCB ASSEMBLY:,REV.0X

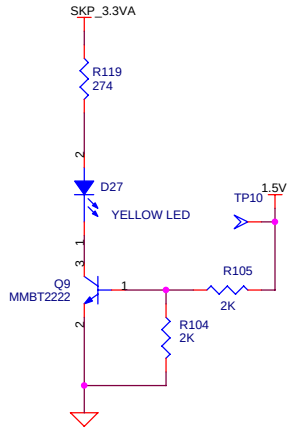
Title	AFS System Supervisor Board	
Size C	Document Number <Doc>	Rev A
Date: Wednesday, September 13, 2006	Sheet 1 of 19	

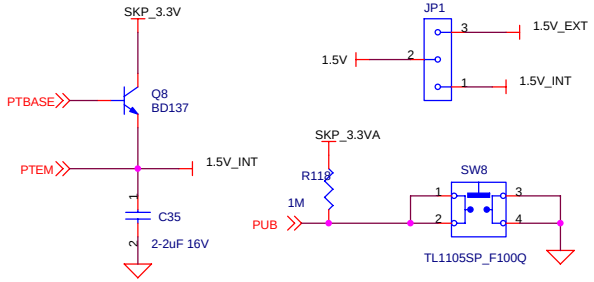
Analog and Digital GND







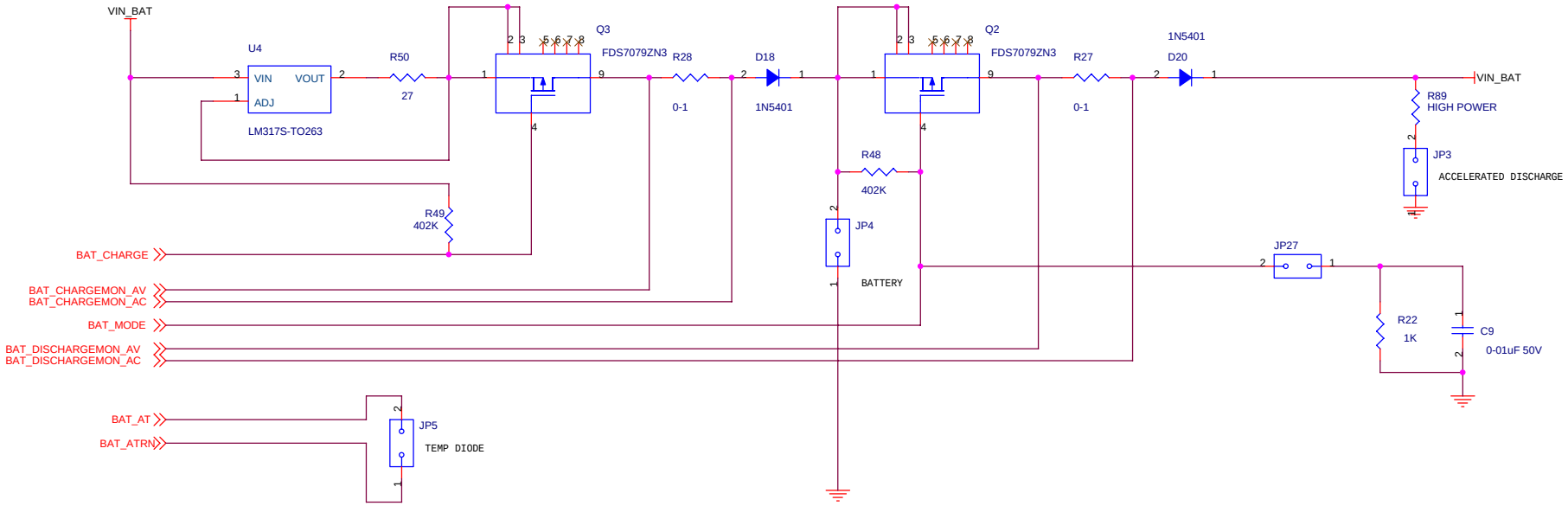




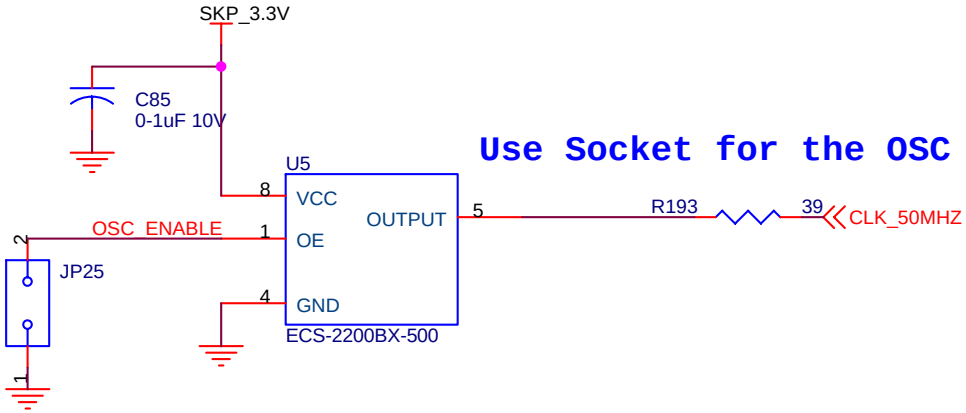
1.5V @ 2A (Max)

One shot pulse generator for RESET
Depolulate after prototype checks

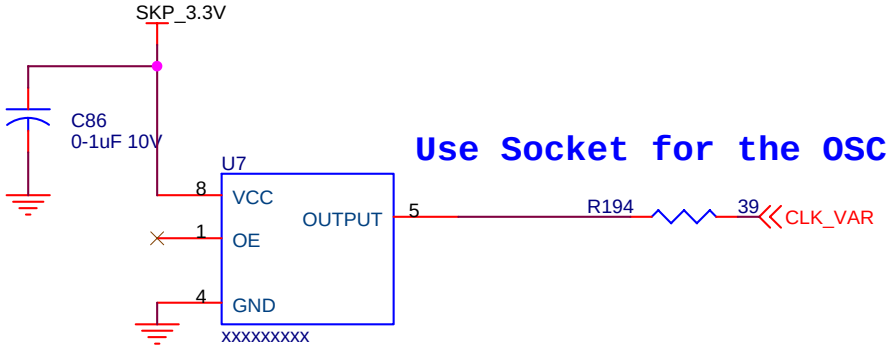
Title	M7AFS System Manager Board	
Size B	Document Number SK Power Supply	Rev A
Date: Wednesday, September 13, 2006	Sheet 2 of 19	



Title	M7AFS System Manager Board	
Size B	Document Number Smart Battery Operation	Rev A
Date: Wednesday, September 13, 2006	Sheet 3 of 19	



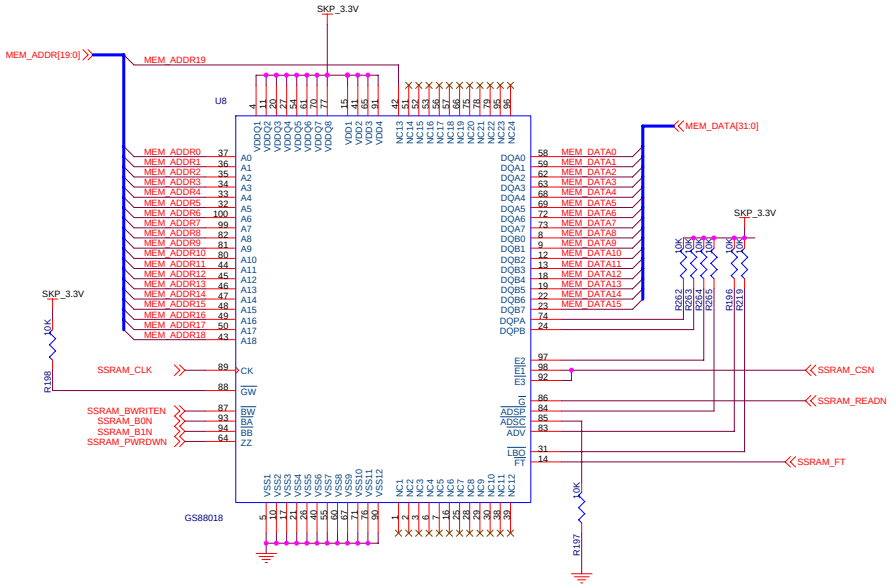
Use Socket for the OSC



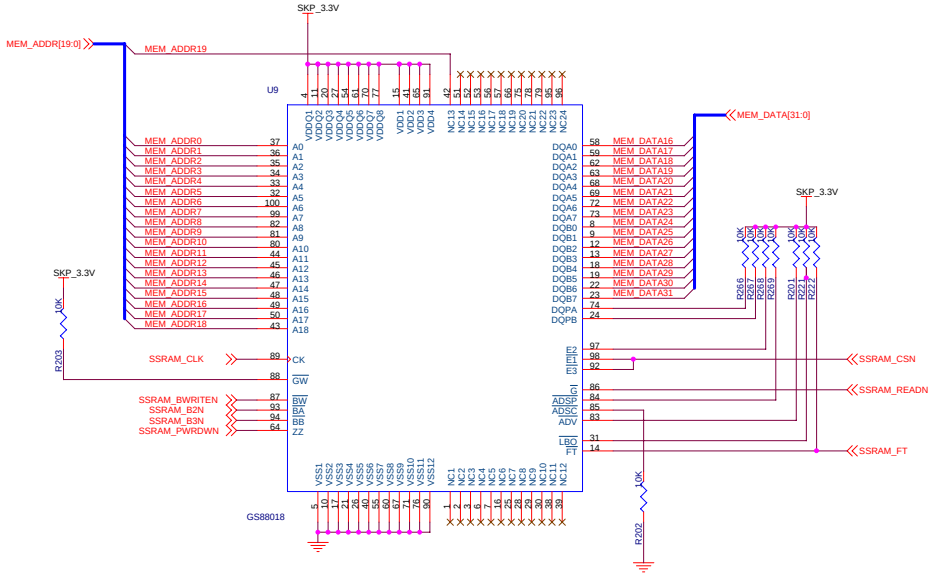
Use Socket for the OSC

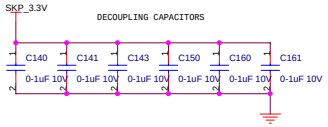
Title: M7AFS System Manager Board		
Size: A	Document Number: Clocks	Rev: A
Date: Wednesday, September 13, 2006	Sheet 4 of 19	

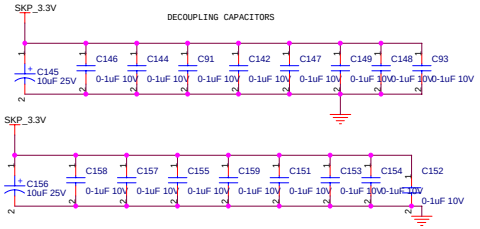
SSRAM 512K/1M * 16
816018 - 1M
88018 - 512k



SSRAM 512K/1M *
16
816018 - 1M
88018 - 512k

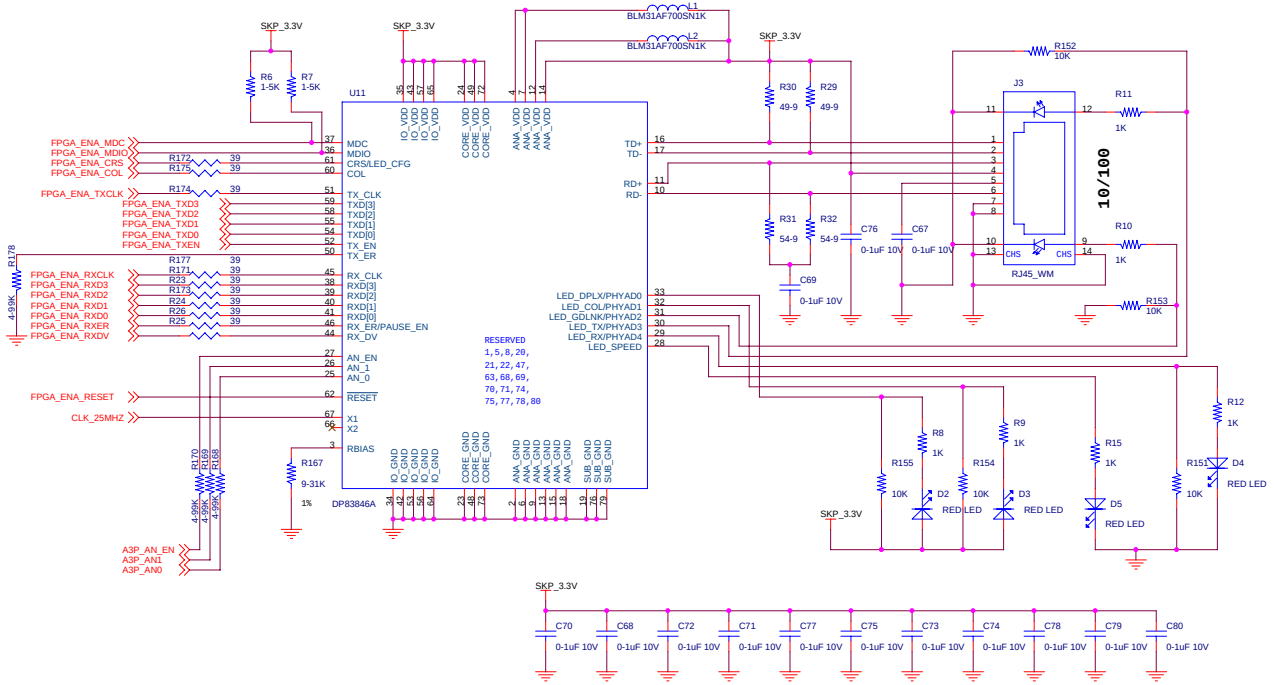


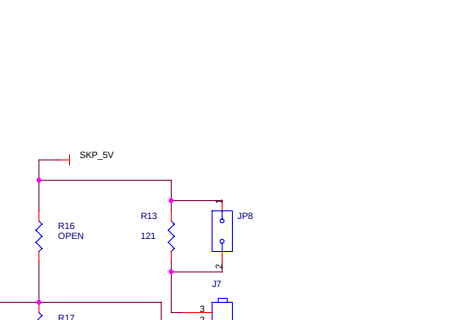




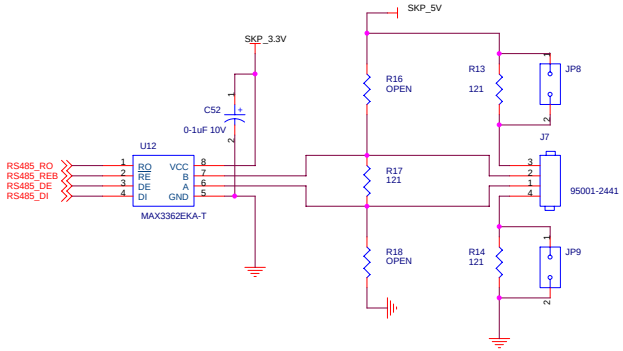
Title	M7AFS System Manager Board		
Size C	Document Number SRAM Memory Block		Rev A
Date: Wednesday, September 13, 2006	Sheet 5 of 19		

10/100 Ethernet PORT

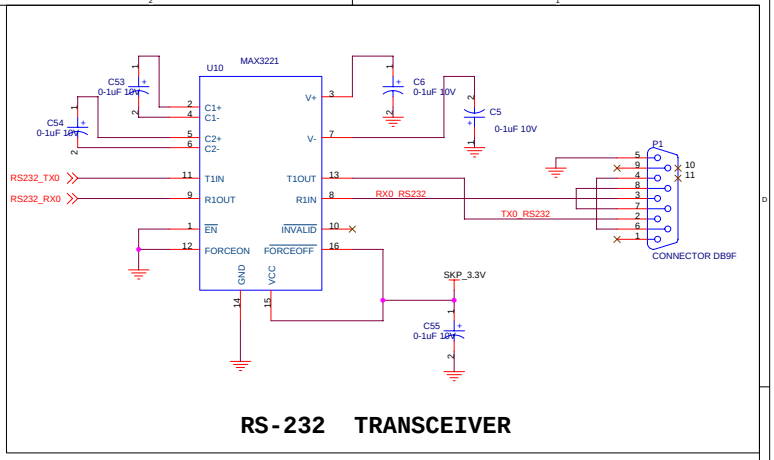




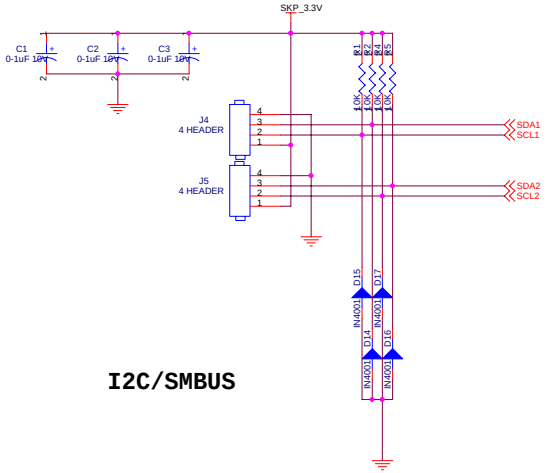
AN_EN	AN1	AN0	Forced Mode
0	0	0	10BASE-T, Half-Duplex
0	0	1	10BASE-T, Full-Duplex
0	1	0	100BASE-TX, Half-Duplex
0	1	1	100BASE-TX, Full-Duplex
AN_EN	AN1	AN0	Advertised Mode
1	0	0	10BASE-T, Half/Full-Duplex
1	0	1	100BASE-T, Half/Full-Duplex
1	1	0	10BASE-T, Half-Duplex 100BASE-TX, Half-Duplex
1	1	1	10BASE-T, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex



RS485 2 WIRE System Transceiver



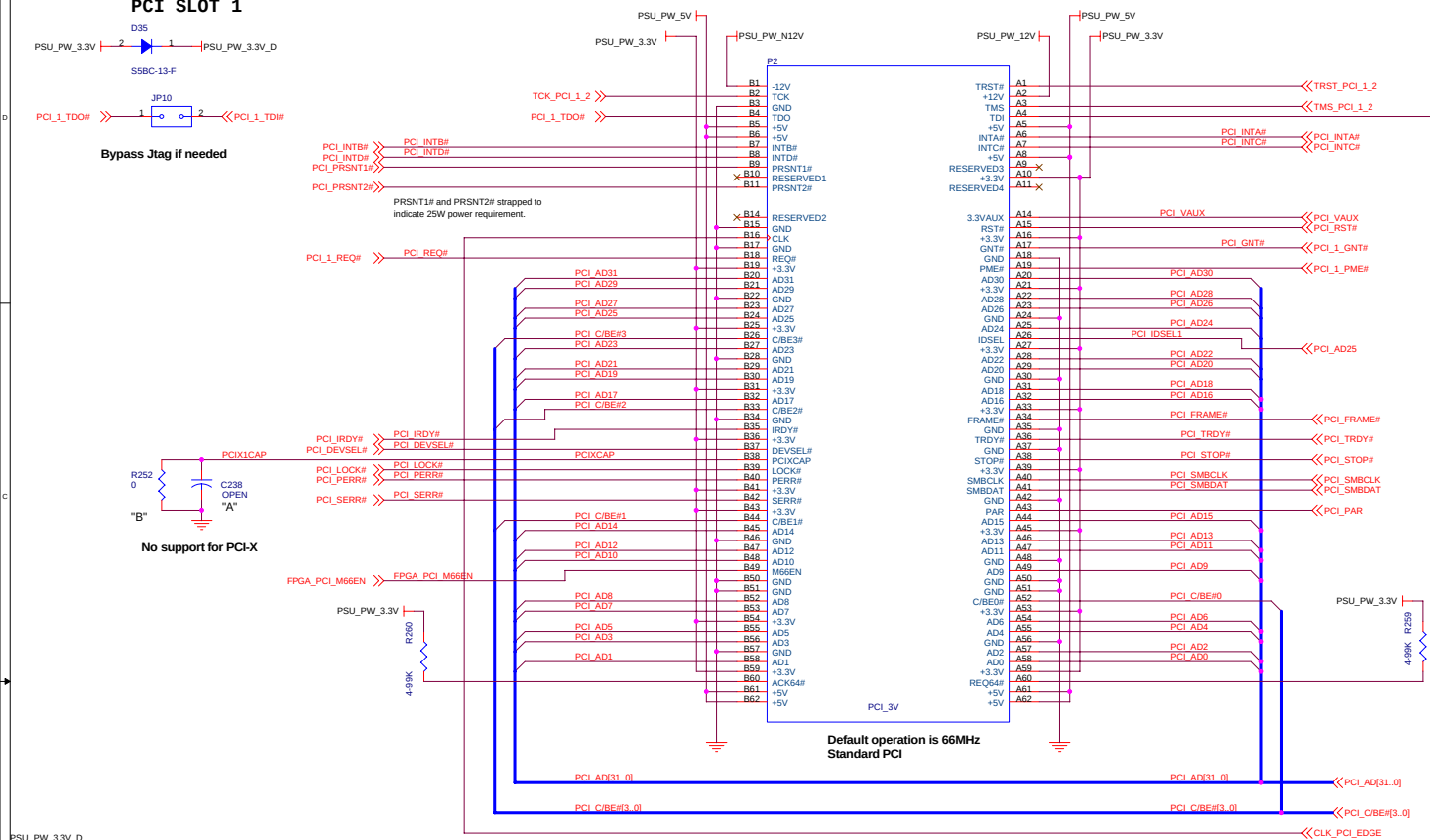
RS-232 TRANSCEIVER

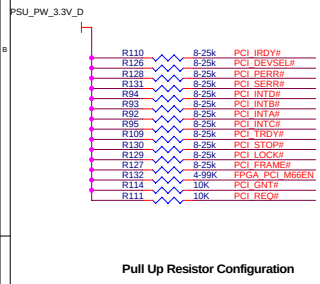


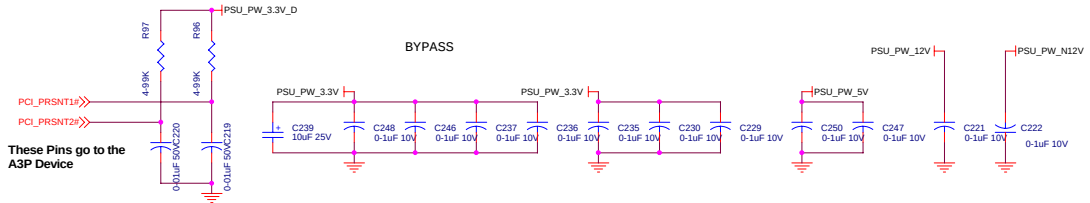
I2C/SMBUS

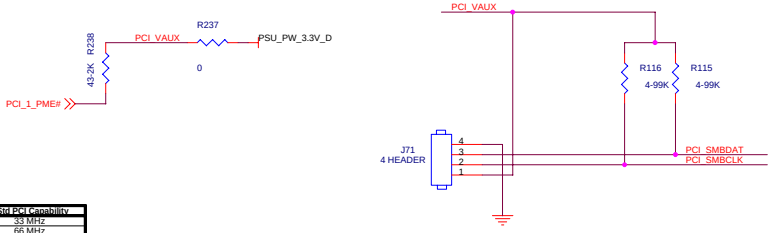
Title	M7AFS System Manager Board
Size C	Document Number Ethernet, SMBus, RS232, RS485
Rev A	
Date: Wednesday, September 13, 2006	Sheet 6 of 19

PCI SLOT 1









A	B	C	PCI-X Capability	Std PCI Capability
empty	0 ohm resistor	0 ohm resistor	Not capable	33 MHz
empty	0 ohm resistor	0.01uF capacitor	Not capable	66 MHz
10k ohm resistor	0.01uF capacitor	0 ohm resistor	PCI-X 66 MHz	33 MHz
10k ohm resistor	0.01uF capacitor	0.01uF capacitor	PCI-X 66 MHz	66 MHz
empty	0.01uF capacitor	0 ohm resistor	PCI-X 133 MHz	33 MHz
empty	0.01uF capacitor	0.01uF capacitor	PCI-X 133 MHz	66 MHz

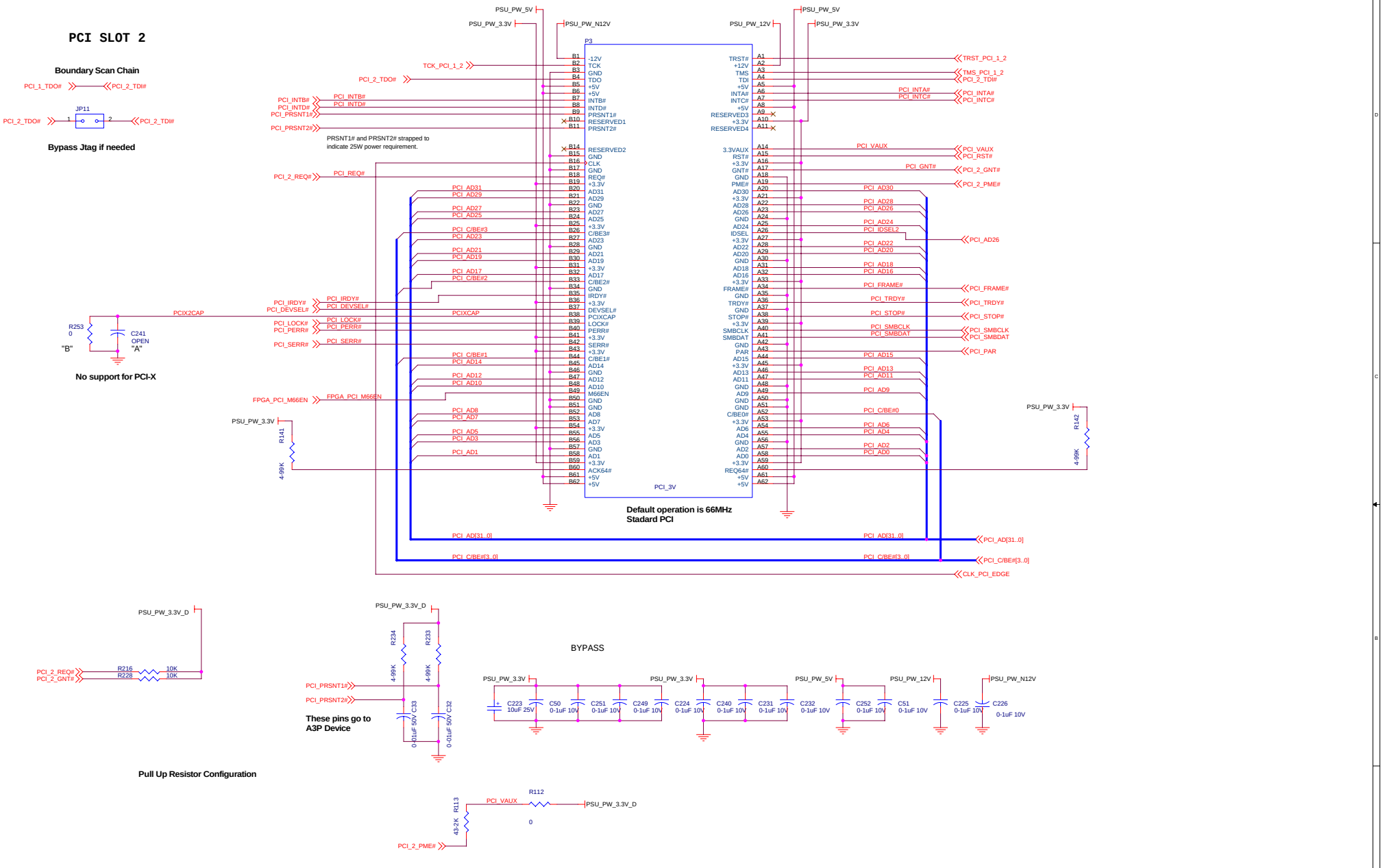
Default: A = empty, B = 0.01uF, C = 0.01uF for PCI-X 133MHz and Std PCI 66MHz support

Layout: Place M66EN and PCIXCAP resistors and capacitors within 0.25" of the associated pin.

Default: No Resistor
No need for FPGA to select mode
It is defaultly configured for 66MHz Standard PCI

Title	M7AFS System Manager Board
Size: C	Document Number: PCI CONNECTOR 1
Rev: A	
Date: Wednesday, September 13, 2006	Sheet 7 of 19

PCI SLOT 2



A	B	C	PCI-X Capability	Std PCI Capability
empty	0 ohm resistor	0 ohm resistor	Not capable	33 MHz
empty	0 ohm resistor	0.01uF capacitor	Not capable	66 MHz
10k ohm resistor	0.01uF capacitor	0 ohm resistor	PCI-X 66 MHz	33 MHz
10k ohm resistor	0.01uF capacitor	0.01uF capacitor	PCI-X 66 MHz	66 MHz
empty	0.01uF capacitor	0 ohm resistor	PCI-X 133 MHz	33 MHz
empty	0.01uF capacitor	0.01uF capacitor	PCI-X 133 MHz	66 MHz

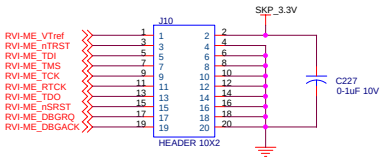
Default: A = empty, B = 0.01uF, C = 0.01uF for PCI-X 133MHz and Std PCI 66MHz support

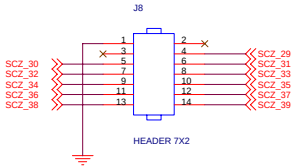
Layout: Place M66EN and PCIXCAP resistors and capacitors within 0.25" of the associated pin.

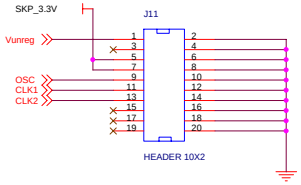
Default: No Resistor
No need for FPGA to select mode
It is defaultly configured for 66MHz Standard PCI

Title	M7AFS System Manager Board	
Size: C	Document Number: PCI Connector 2	Rev: A
Date: Wednesday, September 13, 2006	Sheet 8 of 19	

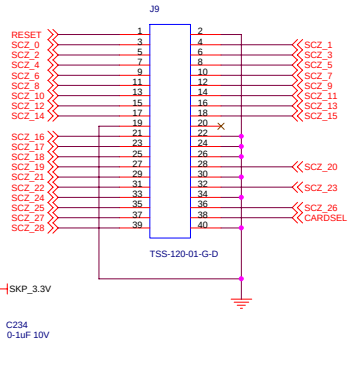
ARM REAL VIEW DEBUGGER

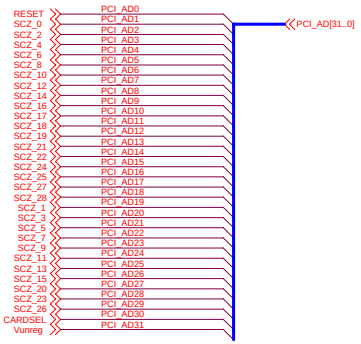


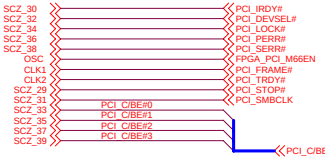


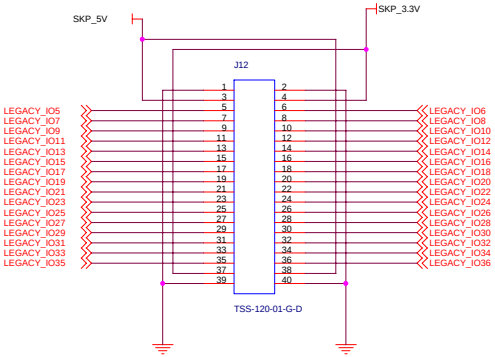


SANTA CRUZ HEADER

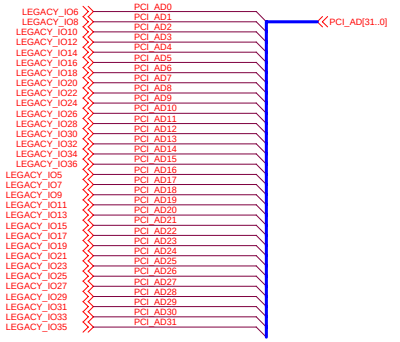






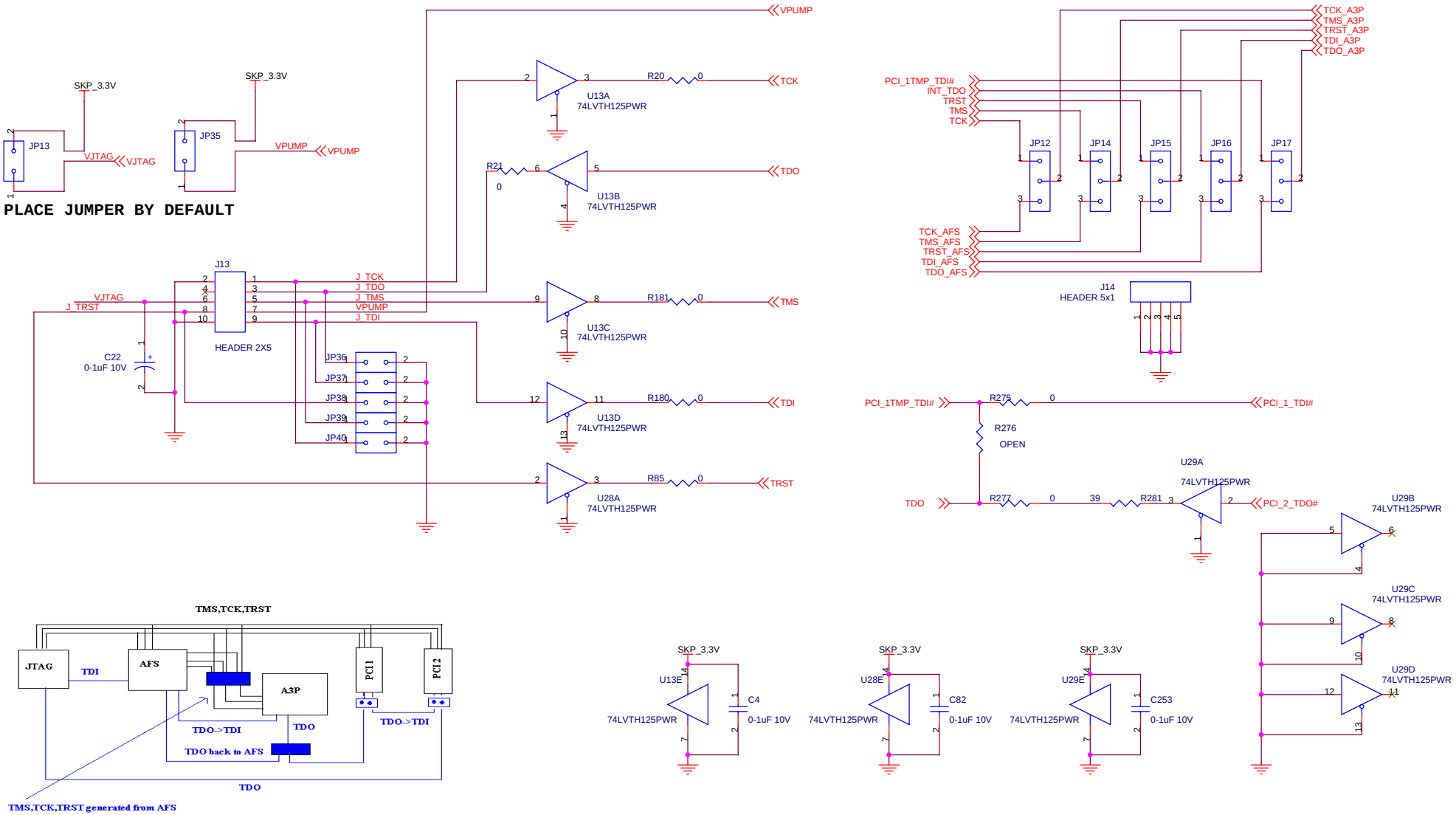


LEGACY CONNECTOR



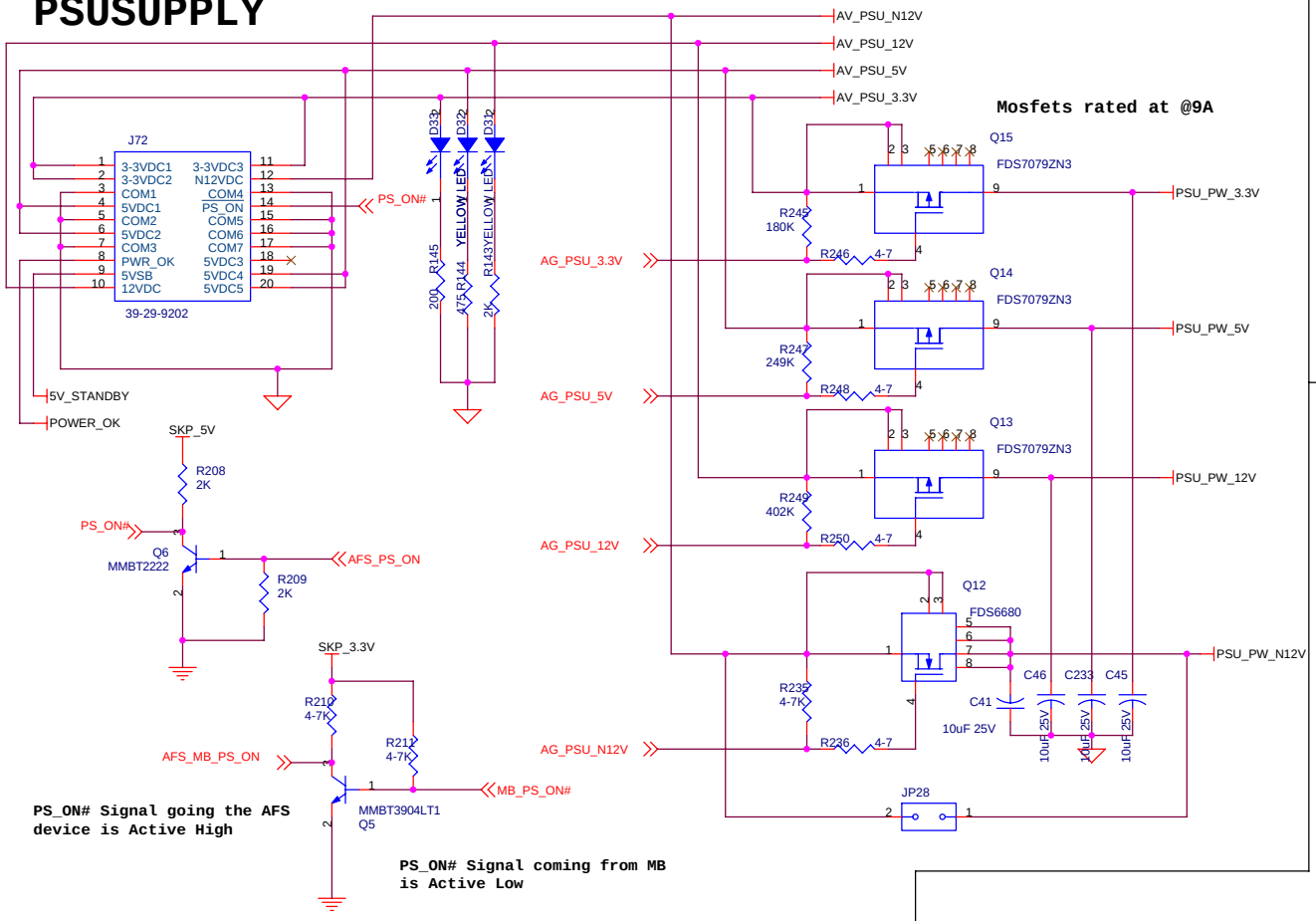
IO SHARING

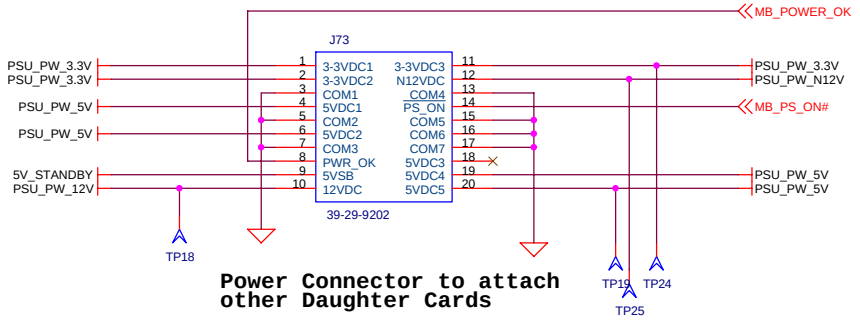
Title	M7AFS System Manager Board	
Size C	Document Number Connectors for ARM, Santa Cruz, Legacy	Rev A
Date: Wednesday, September 13, 2006	Sheet 9 of 19	



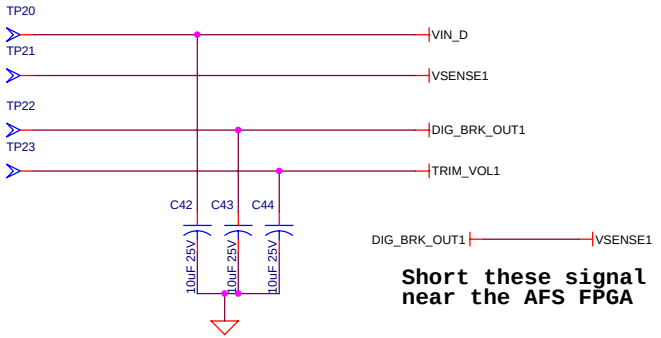
Title	M7AFS System Manager Board	
Size B	Document Number JTAG ISP Programming	Rev A
Date: Wednesday, September 13, 2006	Sheet 10 of 19	

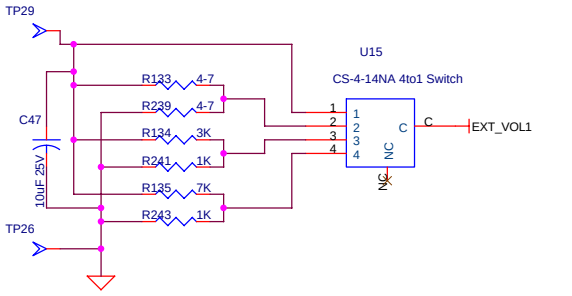
PSUSUPPLY

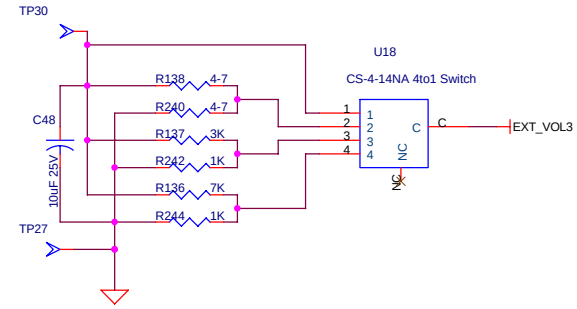


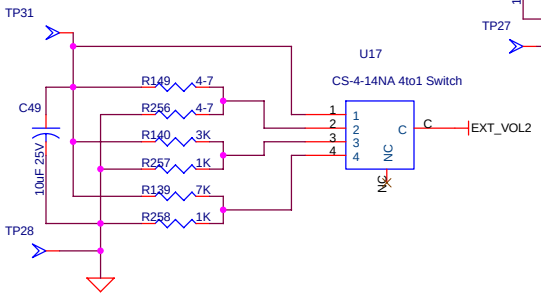


DIG BRICK SUPPLY



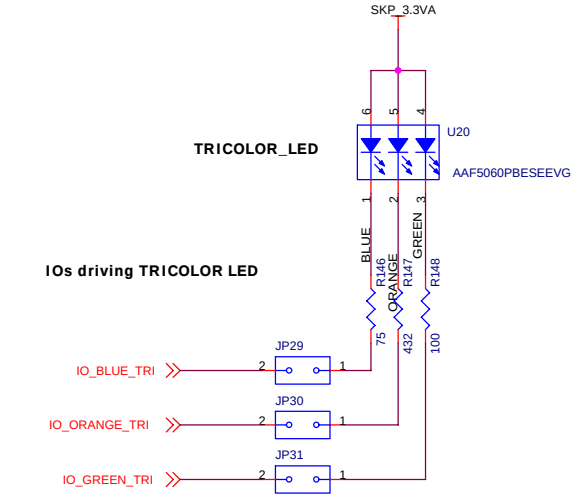


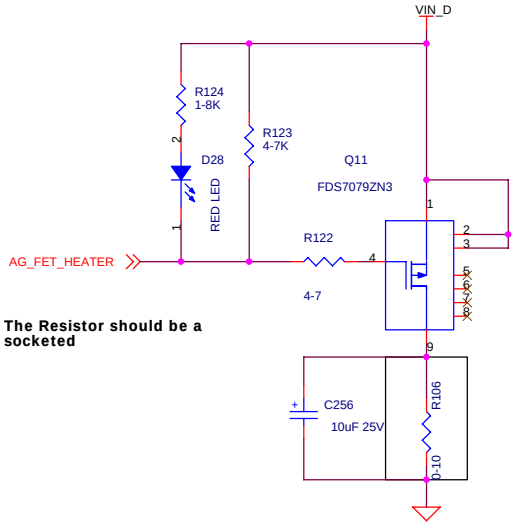




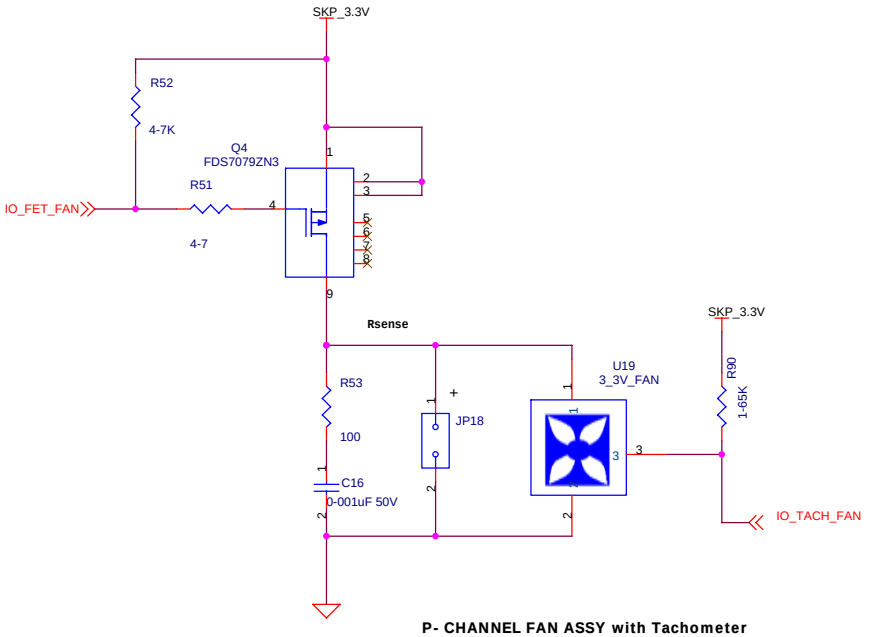
EXT BOARD SUPPLY

Title	M7AFS System Manager Board	
Size B	Document Number PSU_DIG_EXT_SUPPLY	Rev A
Date: Wednesday, September 13, 2006	Sheet 11 of 19	



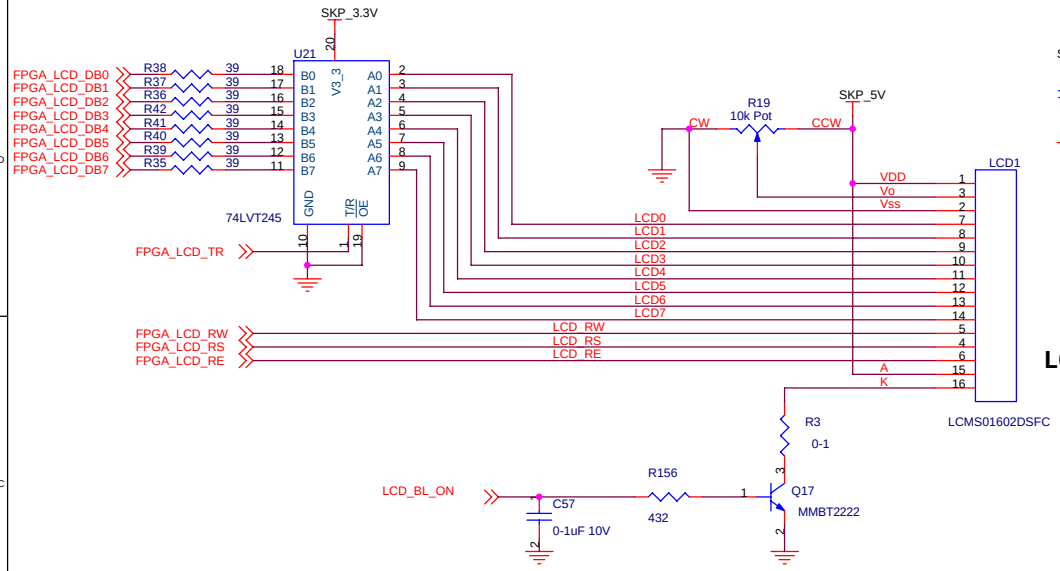


P- CHANNEL HEATER ASSY

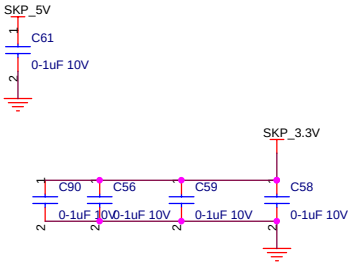


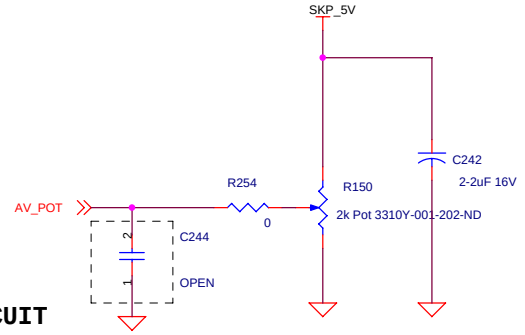
P- CHANNEL FAN ASSY with Tachometer

Title	M7AFS System Manager Board	
Size B	Document Number TRILED, Heater Assy, Fan Assy	Rev A
Date: Wednesday, September 13, 2006	Sheet 12 of 19	



LCD MODULE INTERFACE CIRCUIT



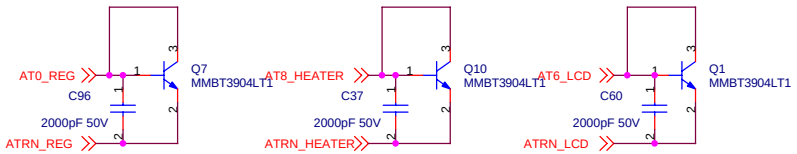


POTENTIOMETER

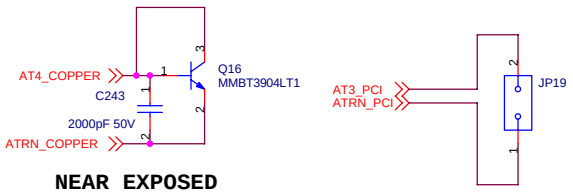
NEAR REGULATORS

NEAR FAN ASSY

NEAR LCD



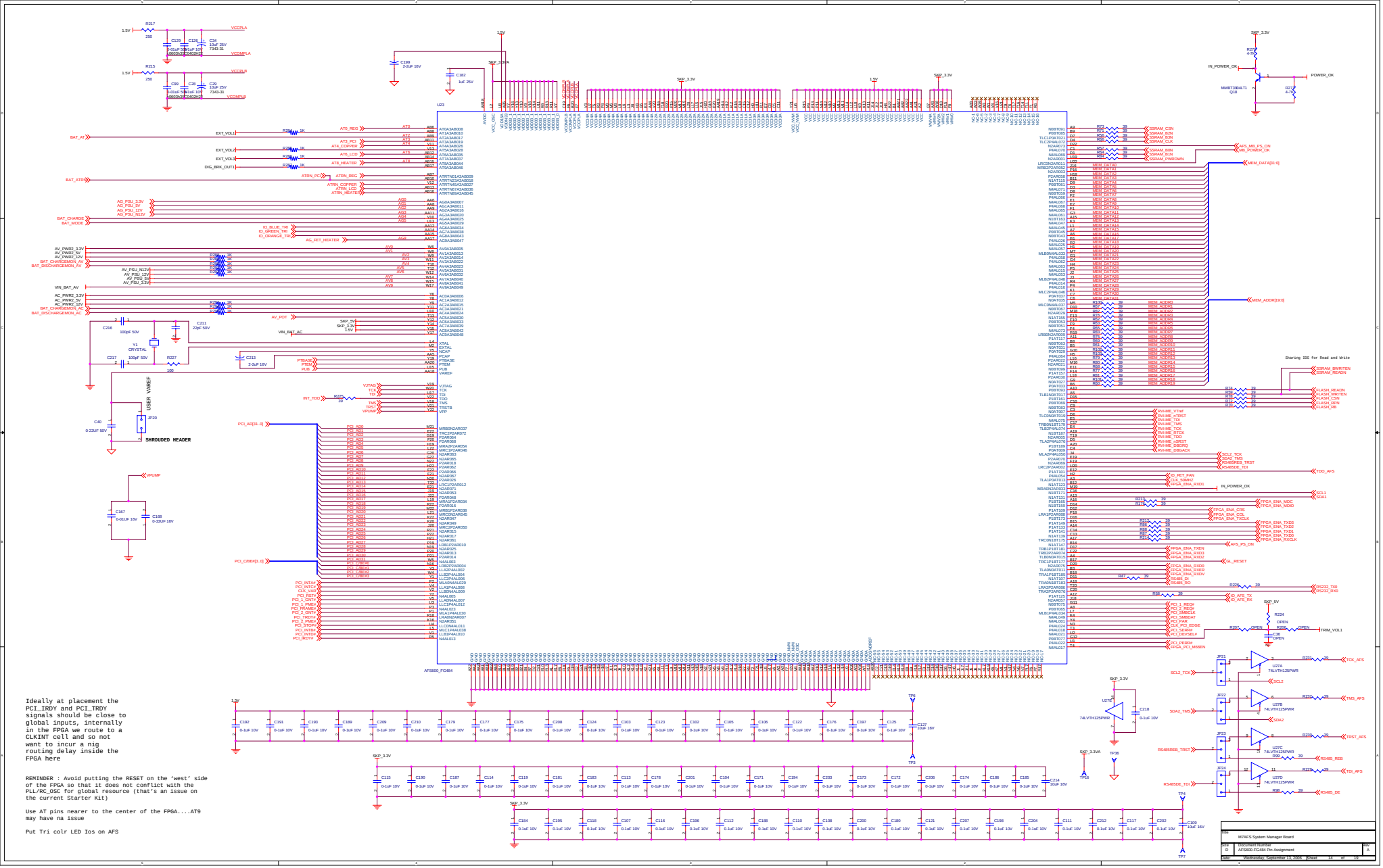
TEMPERATURE DIODE

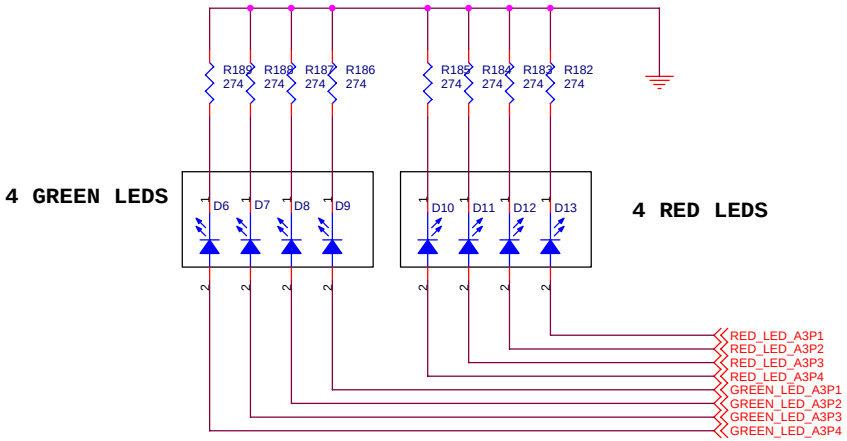


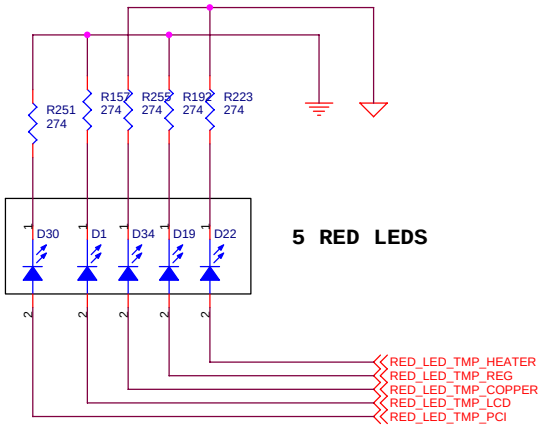
NEAR EXPOSED COPPER PAD

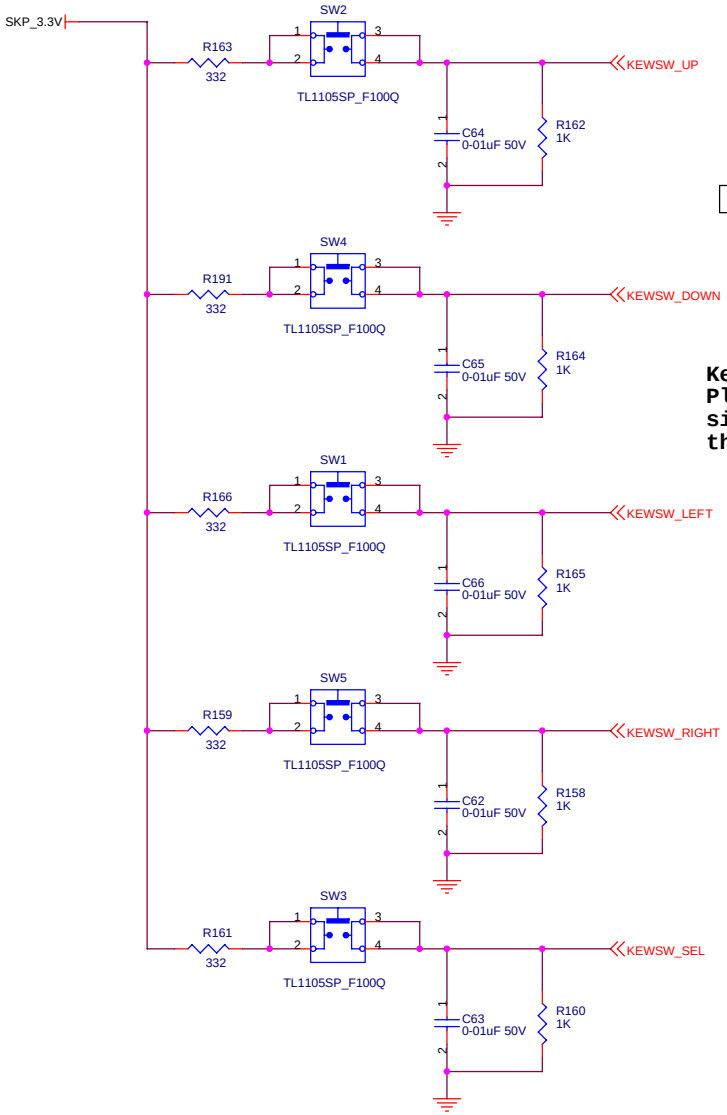
Placed between the two PCI Slots

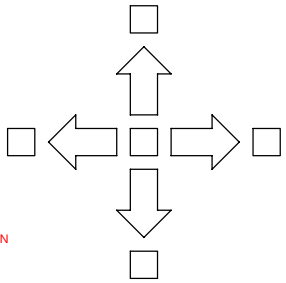
Title	M7AFS System Manager Board	
Size B	Document Number LCD Disply, Potentiometer, Temp Diodes	Rev A
Date: Wednesday, September 13, 2006	Sheet 13 of 19	


Ideally at placement the PCI_IRDY and PCI_TRDY signals should be close to global inputs, internally in the FPGA we route to a CLKINT cell and so not want to incur a nig routing delay inside the FPGA here
REMINDER : Avoid putting the RESET on the 'west' side of the FPGA so that it does not conflict with the PLL/RC_OSC for global resource (that's an issue on the current Starter Kit)
Use AT pins nearer to the center of the FPGA....AT9 may have na issue
Put Tri colr LED Ios on AFS
SHROUDED HEADER
USER VAREF
Sharing IOS For Read and Write
MTAFS System Manager Board
AFS600-FG484 Pin Assignment
Wednesday, September 13, 2006









Key Pad Switch Placement
Please add appropriate silkscreen indicating the arrows

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Size B	Document Number Keypad and Leds	Rev A
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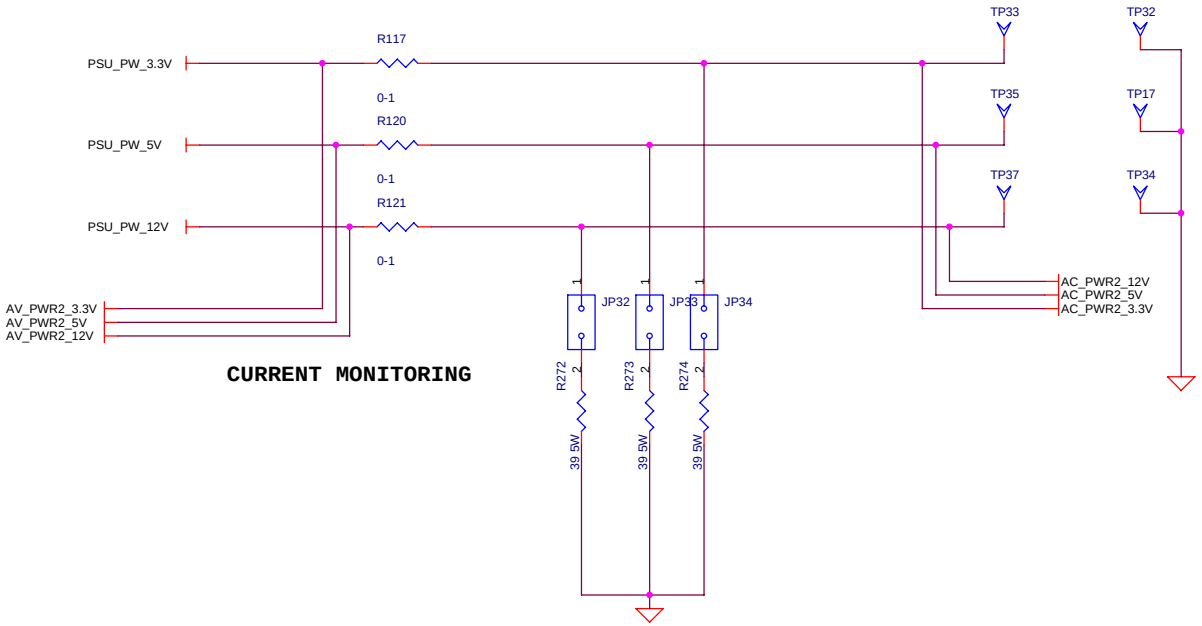
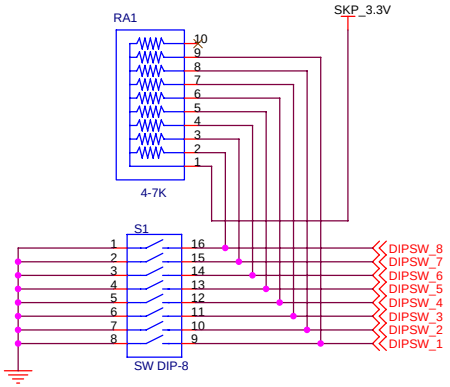


CURRENT MONITORING



DIP SWITCH Configuration

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Size B	Document Number Current Monitoring, DipSwitch	Rev A
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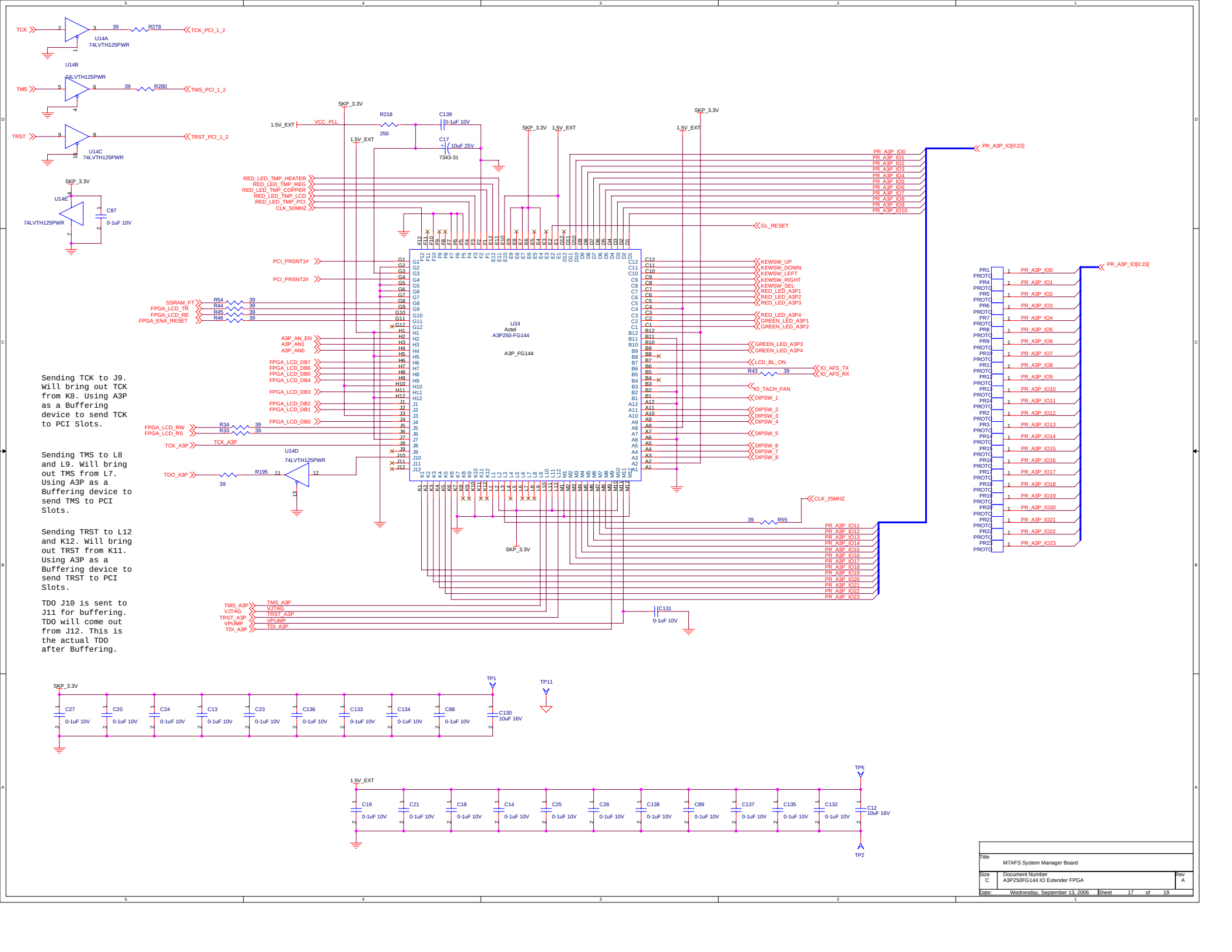
Sending TCK to J9. Will bring out TCK from K8. Using A3P as a Buffering device to send TCK to PCI Slots.
Sending TMS to L8 and L9. Will bring out TMS from L7. Using A3P as a Buffering device to send TMS to PCI Slots.
Sending TRST to L12 and K12. Will bring out TRST from K11. Using A3P as a Buffering device to send TRST to PCI Slots.
TDO J10 is sent to J11 for buffering. TDO will come out from J12. This is the actual TDO after Buffering.
U24
Actel
A3P250-FG144
A3P_FG144
U14A
74LVTH125PWR
U14B
74LVTH125PWR
U14C
74LVTH125PWR
U14D
74LVTH125PWR
U14E
74LVTH125PWR
SKP_3.3V
1.5V_EXT
VCC_PLL
R218
250
C139
0-1uF 10V
C17
10uF 25V
7343-31
TCK
TCK_PCI_1_2
R278
TMS
TMS_PCI_1_2
R280
TRST
TRST_PCI_1_2
C87
0-1uF 10V
RED_LED_TMP_HEATER
RED_LED_TMP_REG
RED_LED_TMP_COPPER
RED_LED_TMP_LCD
RED_LED_TMP_PCI
CLK_50MHZ
PCI_PRSNT1#
PCI_PRSNT2#
SSRAM_FT
FPGA_LCD_TR
FPGA_LCD_RE
FPGA_ENA_RESET
R54
R44
R45
R46
A3P_AN_EN
A3P_AN1
A3P_AN0
FPGA_LCD_DB7
FPGA_LCD_DB6
FPGA_LCD_DB5
FPGA_LCD_DB4
FPGA_LCD_DB3
FPGA_LCD_DB2
FPGA_LCD_DB1
FPGA_LCD_DB0
FPGA_LCD_RW
FPGA_LCD_RS
R34
R33
TCK_A3P
TDO_A3P
R195
GL_RESET
PR_A3P_IO0
PR_A3P_IO1
PR_A3P_IO2
PR_A3P_IO3
PR_A3P_IO4
PR_A3P_IO5
PR_A3P_IO6
PR_A3P_IO7
PR_A3P_IO8
PR_A3P_IO9
PR_A3P_IO10
PR_A3P_IO[0:23]
KEWSW_UP
KEWSW_DOWN
KEWSW_LEFT
KEWSW_RIGHT
KEWSW_SEL
RED_LED_A3P1
RED_LED_A3P2
RED_LED_A3P3
RED_LED_A3P4
GREEN_LED_A3P1
GREEN_LED_A3P2
GREEN_LED_A3P3
GREEN_LED_A3P4
LCD_BL_ON
R43
IO_AFS_TX
IO_AFS_RX
IO_TACH_FAN
DIPSW_1
DIPSW_2
DIPSW_3
DIPSW_4
DIPSW_5
DIPSW_6
DIPSW_7
DIPSW_8
CLK_25MHZ
R55
PR_A3P_IO11
PR_A3P_IO12
PR_A3P_IO13
PR_A3P_IO14
PR_A3P_IO15
PR_A3P_IO16
PR_A3P_IO17
PR_A3P_IO18
PR_A3P_IO19
PR_A3P_IO20
PR_A3P_IO21
PR_A3P_IO22
PR_A3P_IO23
TMS_A3P
VJTAG
TRST_A3P
VPUMP
TDI_A3P
C131
0-1uF 10V
TP1
TP11
C27
C20
C24
C13
C23
C136
C133
C134
C88
C130
10uF 16V
TP5
TP2
C19
C21
C18
C14
C25
C26
C138
C89
C137
C135
C132
C12
10uF 16V
Title
M7AFS System Manager Board
Size
C
Document Number
A3P250FG144 IO Extender FPGA
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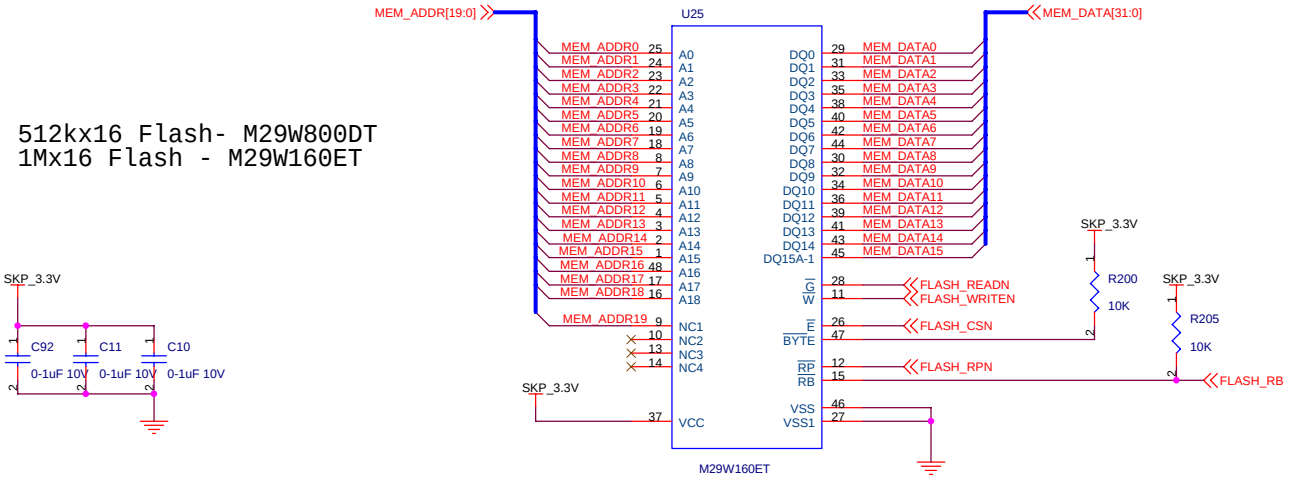
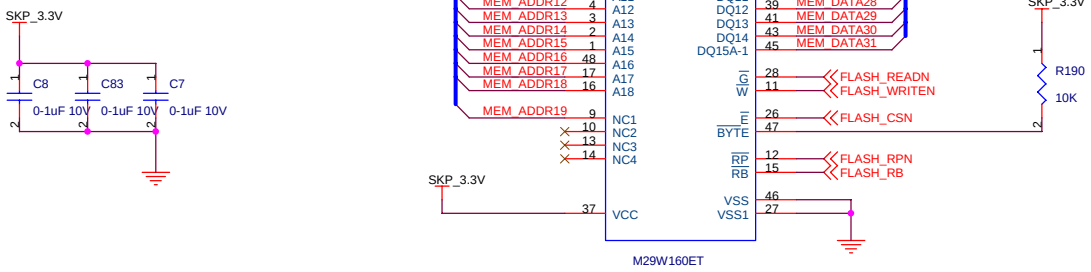
FLASH 512K * 16

512kx16 Flash- M29W800DT
1Mx16 Flash - M29W160ET



FLASH 512K * 16



Title	M7AFS System Manager Board	
Size B	Document Number FLASH Memory	Rev A
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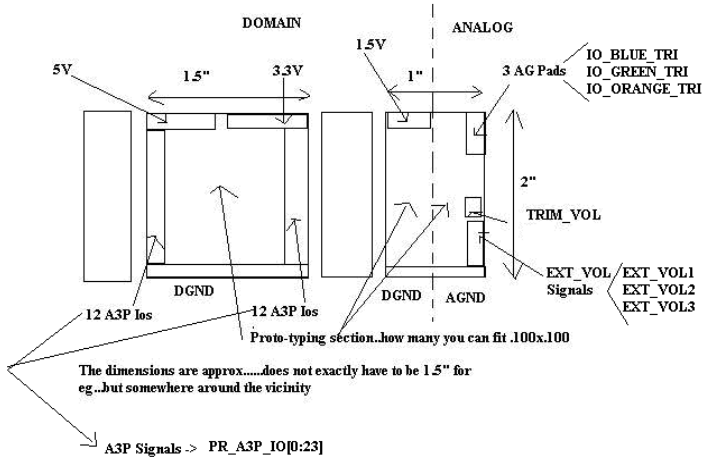
PROTOTYPING AREA



Title	M7AFS System Manager Board	
Size C	Document Number Prototype Area	Rev A
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