Stratix EP1S25 DSP Development Board

December 2004, ver. 1.6 Data Sheet

Features

The Stratix® EP1S25 DSP development board is included with the *DSP Development Kit, Stratix Edition* (ordering code: DSP-BOARD/S25). This board is a powerful development platform for digital signal processing (DSP) designs, and features the Stratix EP1S25 device in the speed grade (-5) 780-pin package.

Components

- Analog I/O
  - Two 12-bit 125-MHz A/D converters
  - Two 14-bit 165-MHz D/A converters
  - Single-ended or differential inputs, and single-ended outputs
- Memory subsystem
  - 2 Mbytes of 7.5-ns synchronous SRAM configured as two independent 36-bit buses
  - 32 Mbits of flash memory
- Configuration options
  - On-board configuration via the 32 Mbits of flash memory, plus the Altera® EPM7064 programmable logic device (PLD)
  - Download configuration data using ByteBlasterMV™ download cables
- Dual seven-segment display
- One 8-pin dual in-line package (DIP) switch
- Three user-definable pushbutton switches
- One 9-pin RS-232 connector
- Two user-definable LEDs
- On-board 80-MHz oscillator
- Single 5-V DC power supply (adapter included)

Debugging Interfaces

- Two Mictor-type connectors for Agilent Technologies logic analyzers
- Several 0.1-inch headers

Expansion Interfaces

- Two connectors for Analog Devices A/D converter daughter cards
- Connector for Texas Instruments Evaluation Module (TI-EVM) daughter cards
- Altera Expansion Prototype Connector
- Footprint for a front panel data port (FPDP)
- Prototyping area

General Description

The Stratix EP1S25 DSP development board provides a hardware platform designers can use to start developing DSP systems based on Stratix devices immediately. Combined with DSP intellectual property (IP) from Altera and Altera Megafunction Partners Program (AMPP^{SM}) partners, users can quickly develop powerful DSP systems. Altera's unique OpenCore®Plus technology allows users to try out these IP cores in hardware prior to licensing them. DSP Builder (version 2.2.1) includes a library for the Stratix EP1S25 DSP development board. This library allows algorithm development, simulation, and verification on the board, all from within The MathWorks MATLAB/Simulink system-level design tools. Additionally, the Stratix DSP development board has a Texas Instruments' EVM (cross-platform) daughter card connector, which enables development and verification of FPGA coprocessors.

Components & Interfaces

Figure 1 shows a top view of the board components and interfaces.

Figure 1. Stratix EP1S25 DSP Development Board Components & Interfaces

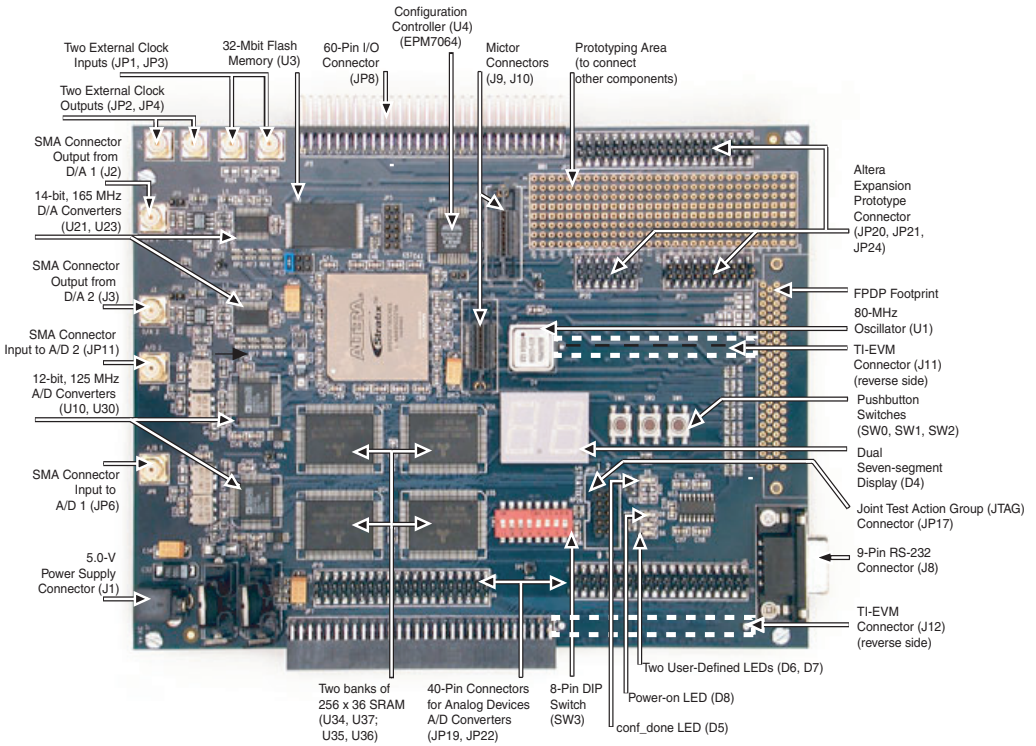


Table 1 describes the components on the board and the interfaces it supports.

Table 1. Stratix EP1S25 DSP Development Board Components & Interfaces (Part 1 of 3)

Component/ Interface	Type	Board Designation	Description
Components			
A/D converters	I/O	U10, U30	The board has two 12-bit 125-MHz A/D converters
D/A converters	I/O	U21, U23	The board has two 14-bit 165-MHz D/A converters
2 MBytes SRAM	Memory	U34, U37	The board has 2 MB of 7.5-ns synchronous SRAM configured as two independent 36-bit buses.

Table 1. Stratix EP1S25 DSP Development Board Components & Interfaces (Part 2 of 3)

Component/ Interface	Type	Board Designation	Description
32 Mbits of flash	Memory	U3	The board has 32 Mbits of flash memory.
SMA external clock input connectors	Input	JP1, JP3	The board has two SMA connector inputs connected to clocks, and terminated in 50 Ω.
SMA external clock output connectors	Output	JP2, JP4	The board has two SMA connector outputs with a source impedance of 50 Ω.
Dual seven-segment display	Display	D4	The board has a dual seven-segment display.
DIPswitch	I/O	SW3	The board has eight DIP switches, which are user-definable as logic inputs.
Pushbutton switches	I/O	SW0, SW1, SW2	The board has three pushbutton switches, which are user-definable as logic inputs.
User-defined LEDs	Display	D6, D7	The board has two user-definable LEDs.
Power-on LED	Display	D8	The board has an LED that illuminates when power is supplied to the board.
conf_done LED	Display	D5	The board has an LED that illuminates upon successful configuration of the Stratix device.
RS-232 connector	I/O	J8	The board has a DB9 connector, which is configured as a DTE serial port. The interface voltages are converted to 3.3-V signals and brought to the Stratix device, which must be configured to generate and accept transmissions.
On-board 80-MHz oscillator	Clock	U1	The board has a socked on-board 80-MHz oscillator.
Single 5.0-V DC power supply	Input	J1 (adapter)	A 5.0-V DC power supply and a board adapter is included.
User I/O pins	I/O	JP7, JP8	The board has ninety general-purpose I/O pins on the 0.1-inch headers (45 on JP8; 45 on JP7). The Stratix pins that drive the JP8 header also drive headers JP20, JP21, and JP24. Similarly, the Stratix pins that drive the JP7 header also drive headers JP19, and JP22.
Debugging Interfaces			
Mictor connectors	I/O	J9, J10	The board has two Mictor headers, each connected to 33 Stratix pins (32 data, 1 clock) for use with an external logic analyzer.
Expansion Interfaces			
Analog Devices connector *(1)*	Expansion	JP19, JP22	The board provides an interface to Analog Device's A/D converters via two 40-pin connectors.
TI-EVM connectors	Expansion	J11, J12	The board provides an interface to the TI-EVM. The connectors can be found on the reverse side of the board, as shown in Figure 1.

Table 1. Stratix EP1S25 DSP Development Board Components & Interfaces (Part 3 of 3)

Component/ Interface	Type	Board Designation	Description
Altera Expansion Prototype Header	Expansion	JP20, JP21, JP24	The board provides a custom interface to Altera expansion cards via a 74- pin header.
FPDP Footprint	Expansion	J4	Four rows of pins comprise a footprint for an FPDP, which can be added to the board.
Prototyping area	Expansion	N/A	The board provides a grid of plated through-holes on 0.1-inch centers. Thirty Stratix I/O pins are connected to the grid.

Note to Table 1:

(1) The two debug headers designated in this table can be used to interface to Analog Devices A/D converter evaluation boards. They are designated as JP19 and JP22, and interface to Analog Devices AD6645/9433/9430 external A/D converters. Note that the JP19 and JP22 headers share Stratix pins with JP7.

Environmental Requirements

The Stratix EP1S25 DSP development board must be stored between –40° C and 100° C. The recommended operating temperature is between 0° C and 55° C.

The Stratix EP1S25 DSP development board can be damaged without proper anti-static handling.

Using the Board

When power is applied to the board, the Power On LED illuminates. At this time, the Stratix device is automatically configured and, upon successful configuration, the `conf_done` LED illuminates.

JP18 allows the user to load one of two Stratix configuration images upon power-up. If the jumper on JP18 is not present, the *factory configuration* loads. If the jumper is present, the *user configuratio*n loads. See "Non-Volatile Configuration" on page 7 for more details.

To configure the board with a new design, the designer should perform the following steps, explained in detail in this section.

1. Apply power to the board.
2. Configure the Stratix device.

Apply Power

Apply power to the board by connecting the 5.0-V DC power supply adapter, provided in the *DSP Development Kit*, to connector J1 (see Figure 1 on page 3). All of the board components draw power either directly from this 5.0-V supply, or through the 3.3-V and 1.5-V regulators that are powered from the 5.0-V supply.

The 3.3-V supply provides V_{CCIO} to the Stratix device and LVTTL board components. The 1.5-V supply provides V_{CCINT} to the Stratix device.

When power is applied to the board, the Power On LED (D9) illuminates.

CAUTION

The Stratix EP1S25 device, the A/D and D/A converters, and the board's heat sink become hot as the board is used. Because their surface temperature may significantly increase, **do not touch these devices while there is power applied to the board**.

Configure the Stratix Device Directly

You can configure the Stratix device directly, without turning off power, using the Quartus® II software and the ByteBlasterMV cable, as follows.

1. Attach the cable to JP17.
2. Open a Quartus II SRAM Object File (**.sof**), which launches the Quartus II Programmer.
3. Select **ByteBlasterMV** as the hardware.
4. Set the mode to **JTAG**.
5. Click **Start**.

On successful configuration, the **conf_done** LED (D5) illuminates.

For instructions on how to use the ByteBlasterMV cable, see the Quartus II Help.

Non-Volatile Configuration

The Stratix device is SRAM-based, therefore, the designer must reconfigure it each time power is applied to the Stratix DSP development board. For designers who want to power up the board and have a design immediately present in the Stratix device, the board has a non-volatile configuration scheme. This scheme consists of a configuration controller (U4), which is an Altera EPM7064 PLD, and flash memory. The configuration controller device is non-volatile (that is, it does not lose its configuration data when the board is powered down) and it comes factory-programmed with logic that configures the Stratix EP1S25780C5 device (U2) from data stored in flash (U3) on power-up. Upon power-up, the configuration controller begins reading data from the flash memory. The flash memory, Stratix device, and configuration controller are connected so that data from the flash configures the Stratix device in fast passive-parallel mode.

Configuration Data

The Quartus II software can (optionally) produce Hexadecimal Output Files (**.hexout**) that are suitable for download and storage in the flash memory as configuration data. The designer can create a **.hexout** file using the Quartus II version 4.2 software in one of the following ways:

- Write a **.hexout** at the end of compilation
- Convert a SOF to a **.hexout**

Write a .hexout at the End of Compilation

To set up a project so that the Quartus II software writes a **.hexout** at the end of compilation, perform the following steps:

1. Choose **Settings** (Assignments menu).
2. Click **Device** under **Compiler Settings**.
3. Click **Device and Pin Options**.
4. Click the **Programming Files** tab.
5. Turn on the **Hexadecimal (Intel-Format) Output File (.hexout)** option. With this option turned on, the Quartus II software generates a **.hexout** at the end of a successful compilation.

Convert a .sof to a .hexout

The designer can convert a **.sof** file into a **.hexout** by performing the following steps in the Quartus II software:

1. Choose **Convert Programming Files** (File menu).
2. Under **Output programming file**, choose **Hexadecimal (Intel-Format) Output File for SRAM (.hexout)** from the **Programming file type** list box.
3. Specify an output file name in the **File name** box. The default is **output_file.hexout**.
4. Click **SOF Data** under **Input files to convert**.
5. Click **Add File**.
6. Browse to the **.sof** to convert and click **OK**. The Quartus II software converts the file and saves the output file to the directory specified.

Intel-format **.hexout** contain data that is not actually written to the flash memory. The **Write2Flash** executable file (provided in the <*installation directory*>**/utilities/Flash_Programmer** directory) parses the **.hexout** and creates a **.hexout.flash** that contains the data to be written to flash memory. The designer can then send this file serially to the board via an RS-232 cable and write it to flash memory by the factory configuration as described in "Factory & User Configurations".

Factory & User Configurations

The configuration controller can manage two separate Stratix device configurations (**.hexout**) stored in flash memory, a *user configuration* and a *factory configuration*. Upon power-up the configuration controller reads one of the two (user or factory) configurations from the flash memory and into the Stratix device. The user can select which configuration loads into the Stratix device by adding or removing the jumper on JP18. If the jumper is present on JP18, the controller configures the Stratix device with the user configuration. If the jumper is removed, the factory configuration is loaded.

The factory-provided user configuration, which loads into flash if the JP18 jumper is present and power is applied to the board, is a simple design that exercises the seven segment display. Switches 1 and 2 (SW1 and SW2) on the board control what/how the display is exercised. It either counts in hex from 00 to FF and loops or it illuminates the edges of the seven segment display in a round-robin fashion. SW1 switches back

and forth between the counter or the edge illuminations, and SW2 controls the speed of the counting or the illuminating, depending on which one is currently running. This test design allows the designer to verify that the board is working correctly with a user configuration.

The factory configuration contains a design that allows the designer to write a user configuration to the flash memory. To download the Quartus II-generated **.hexout** to the board, use the Altera-provided **Write2Flash.exe** utility, which is located in the **Flash_Programmer** directory. This utility downloads the **.hexout** to the development board via the PC's serial port. If the factory configuration is loaded, it writes the **.hexout** to the flash memory. When the jumper at JP18 is in place and the power to the board is cycled, the user configuration is read from the flash memory and written to the Stratix device.

To download a user configuration into flash memory, perform the following steps:

1. Use the Quartus II software to generate a **.hexout** file as described in "Configuration Data" on page 7.

2. Connect a serial cable from the board to the PC (note whether you are using COM 1 or COM 2).

3. Remove the jumper at JP18 if it is present.

4. Power up the board. The factory configuration is loaded in the Stratix device. The seven segment display should read FF.

5. Press SW1 on the board to erase the previous user configuration from flash memory. The seven-segment display should read 00. It actually counts backwards in hex from the value 20h (32 decimal) to 00. Depending on how fast the configuration erases, you may or may not see the counting.

6. Run the **Write2Flash.exe** utility in the <*installation path*>/**utilities/Flash_Programmer** directory.

7. In the **Write2Flash** user interface, select the **.hexout** to store in flash memory as the user configuration.

8. Select the appropriate COM port (1 or 2).

   The **Region Setting** option must be turned on for PCs that have an operating system with double byte code set (DBCS), or unicode characters. For example, Microsoft Windows uses DBCS, instead of ASCII, for some of its language versions, including Chinese, Korean, and Japanese.

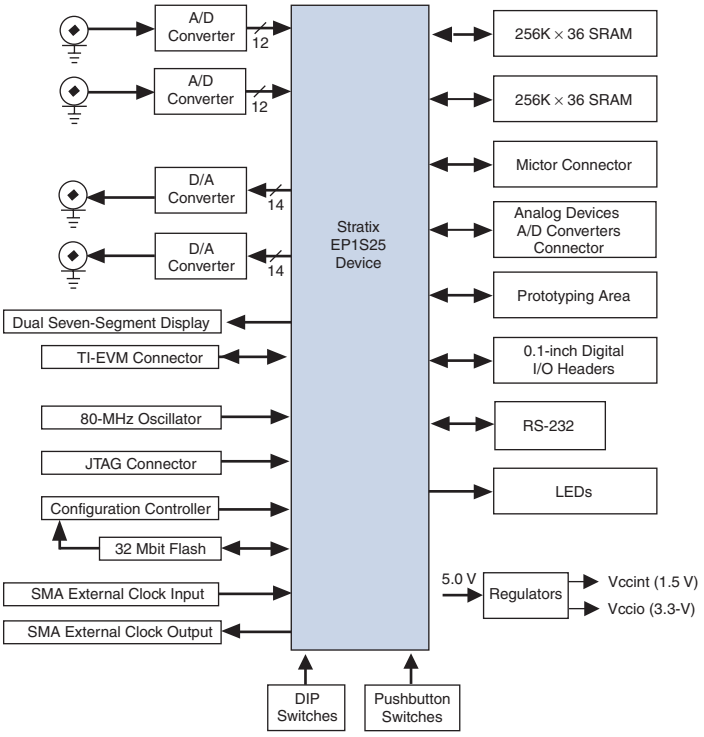
9. Click **Begin**. Transmission begins and takes about 15 minutes. The seven segment display counts when data transmission begins. It counts to the digits FE, and the **Write2Flash** utility reports that it has successfully downloaded the **.hexout**.

10. Ensure that the jumper at JP18 is in place and cycle the power on the Stratix board. The user configuration is loaded in the Stratix device.

Functional Description

This section describes the elements of the Stratix EP1S25 DSP development board. Figure 2 shows a block diagram of the board and, as mentioned earlier in this data sheet, Figure 1 on page 3 shows a photograph of the board indicating names and locations of all components and interfaces.

Figure 2. Stratix EP1S25 Development Board Block Diagram



Power

The 12-layer development board has eight signal layers and four ground/VCC planes. The board is powered from a single, well-regulated 5.0-V supply.

Regulators on the board are used to develop the V_{CCINT} (1.5 V) and V_{CCIO} (3.3 V) voltages. The board includes a Power On LED that indicates the presence of V_{CCIO}.

The following board elements are 3.3 V.

- LEDs
- Switches
- Crystal oscillator

Table 2 presents the specifications for the 5-V power supply, which connects from the wall socket to the DSP development board.

Table 2. Power Supply Specifications

Item	Description
Board reference	N/A (power supply adapter)
Part number	DTS050400UDC-P5-SZ
Device description	Model EPA-201DA-05, 5.0-VDC power supply Input: AC 100 V – 240 V, 45-60VA Output: DC 4A/20W
Manufacturer	CUI
Manufacturer web site	**www.cui.com**

Stratix Device

The EP1S25 device on the board features 25,660 logic elements (LEs) in a fastest-grade (-5) 780-pin FineLine BGA® package. The device has 1,944,576 total RAM bits.

For more information on Stratix devices, see the *Stratix Programmable Logic Device Family Data Sheet*.

Table 3 describes the Stratix device features.

Table 3. Stratix Device Features (Part 1 of 2)

Feature	EP1S25F780-5
Logic elements (LEs)	25,560
M512 RAM Blocks (32 × 18 bits)	224
M4K RAM Blocks (128 × 36 bits)	138
M-RAM Blocks	2
Total RAM bits	1,944,576
DSP Blocks	10
Embedded multipliers (based on 9 × 9)	80
PLLs	6

Table 3. Stratix Device Features (Part 2 of 2)	
Feature	**EP1S25F780-5**
Maximum user I/O pins	597
Package type	780-pin FineLine BGA
Board reference	U1
Voltage	1.5-V internal, 3.3-V I/O

Clocks & Clock Distribution

Table 4 lists the clocks and their signal distribution throughout the board.

Table 4. Clock Distribution Signals		
Signal Name	**Comes From**	**Goes To**
CLK_DEBUGA	Stratix pin Y16 (PLL6_OUT_3n)	J9 pins 5, 6 (Mictor A)
CLK_DEBUGB	Stratix pin K16 (PLL5_OUT_3p)	J10 pins 5, 6 (Mictor B)
CLK_TI_OUT/2	(J11 pin 78) (TI-EVM connector)	Stratix pin P27 (CLK0p)
CLK_DTOA1	Stratix pin AE15 (PLL6_OUT_0n)	U21 pin 28 (D/A1 converter)
CLK_DTOA2	Stratix pin AD15 (PLL6_OUT_0p)	U23 pin 28v (D/A2 converter)
CLK_SRAM1	Stratix pin W14 (PLL6_OUT_1p)	U34 pin 89 U35 pin 89 (SRAM Bank 1)
CLK_SRAM2	Stratix pin W15 (PLL6_OUT_1n)	U36 pin 89 U37 pin 89 (SRAM Bank 2)
CLK_OPT_ATOD	Stratix pin E15 (PLL5_OUT_0p)	JP23 pin 4 *(1)*
CLK_OSC	80-MHz oscillator	Stratix pin K17 (CLK14p) Stratix pin AC17(CLK4p) JP23 pin 2 *(1)*
CLK_SMA_IN1	JP1	Stratix pin M17 (CLK15p) Stratix pin AA17 (CLK5p) JP23 pin 6 *(1)*
CLK_SMA_IN2	JP3	Stratix pin L17 (CLK15n) Stratix pin Y17 (CLK5n)
CLK_SMA_OUT1	Stratix pin C15 (PLL5_OUT_2p)	JP2
CLK_SMA_OUT2	Stratix pin B15 (PLL5_OUT_2n)	JP4
CLK_EVALIO_IN44	JP7 pin 59	Stratix pin P25 (CLK1P)
CLK_EVALIO_OUT44	Stratix pin W16 (PLL6_OUT_3p)	JP8 pin 59, JP21 pin 11

Note to Table 4:

(1) JP23 controls which clock is routed to the A/D converters after it passes through a differential LVPECL buffer. See Table 10 on page 18 for details.

The Stratix EP1S25 DSP development board can obtain a clock source from one or more of the following sources:

- The on-board crystal oscillator
- An external clock (through an SMA connector or Stratix pin)

The board can provide independent clocks from both the enhanced and fast PLLs to the A/D converters, the D/A converters, and the other components that require stable clock sources.

To implement this concept, the enhanced PLL5-dedicated pins drive the A/D converters and associated functions, and the enhanced PLL6-dedicated pins drive the D/A converters and associated functions.

Figure 3 is a diagram of each clock and their distribution throughout the board.

Figure 3. Clock Distribution

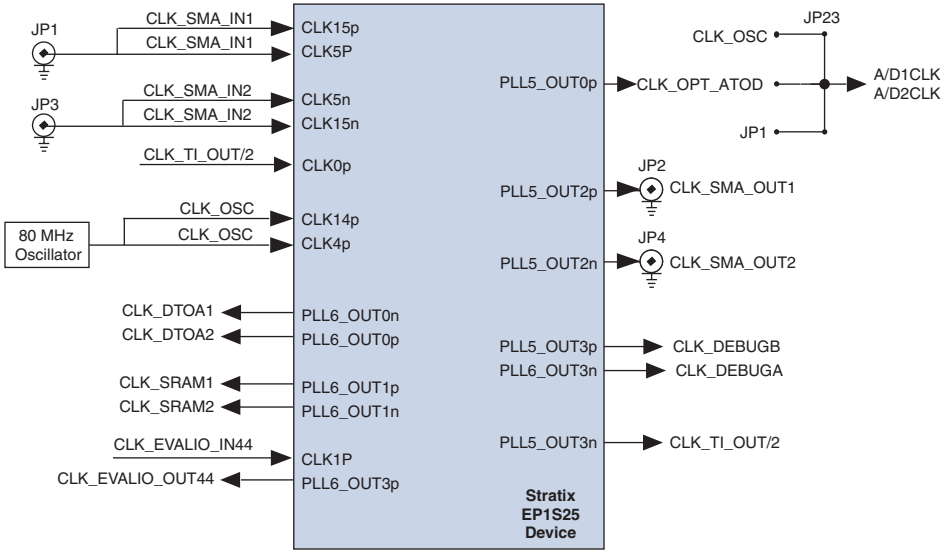


Table 5 lists the reference information for the 80-MHz on-board oscillator.

Table 5. 80-MHz On-Board Oscillator Reference

Item	Description
Board reference	U1
Part number	ECS-2200B
Device description	Oscillator
Manufacturer	ECS Inc.
Manufacturer web site	**www.ecsxtal.com**

Board Components

The following sections describe the development board components.

Switch Inputs

The board has eight DIP switches and three pushbutton switches, which are user-definable as logic inputs, as shown in Table 6. Each pushbutton signal is defined as a logic 1 when in its normal state; when pressed, it becomes a logic 0; when released it goes back to logic 1.

The DIP switches drive a logic 1 to the Stratix device when in the off position, and a logic 0 into the Stratix device when in the on position.

Table 6. Switch Pin-Outs

Signal Name	Stratix Pin
Pushbuttons	
SW0	F24
SW1	N26
SW2	N25
DIP Switches	
SW3p1	N24
SW3p2	N23
SW3p3	N22
SW3p4	N21
SW3p5	N20
SW3p6	N19
SW3p7	F25
SW3p8	M26

Dual Seven-Segment Display & LEDs

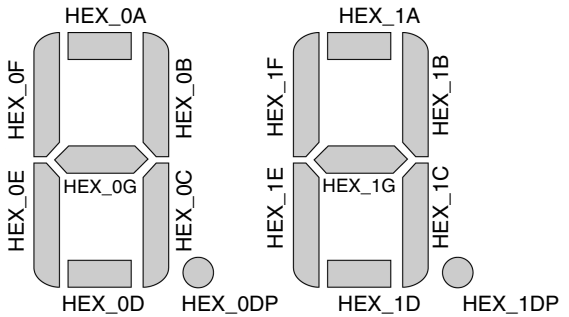
A dual seven-segment display and two LEDs are provided as shown in Table 7. The segments and LEDs illuminate if the Stratix pin to which they are connected drives a logic-0. They will appear unlit when the Stratix pin to which they are connected drives a logic-1.

Table 7. Seven Segment Display & LED Pin-Outs

Signal Name	Stratix Pin
Dual Seven Segment Display	
HEX_0A	L19
HEX_0B	L20
HEX_0C	L22
HEX_0D	L24
HEX_0E	L23
HEX_0F	D24
HEX_0G	L18
HEX_0DP	L21
HEX_1A	L26
HEX_1B	E16
HEX_1C	M18
HEX_1D	M20
HEX_1E	M21
HEX_1F	L25
HEX_1G	M19
HEX_1DP	F26
LEDs	
LED0	M25
LED1	M24

Figure 4 shows the name allocation of the seven-segment display.

Figure 4. Pin-Out Diagram for the Dual Seven-Segment Display



Serial Interface

The board contains a DB9 connector, which provides a bidirectional RS-232C serial I/O interface. The board contains the transceiver, however the Stratix device must implement the logic controller. Table 8 describes the device used to implement the RS-232C interface.

Table 8. RS-232C Interface Device Reference

Item	Description
Board reference	None
Part number	MAX221E
Device description	RS-232 transceiver
Voltage	3.3 V
Manufacturer	Maxim
Manufacturer web site	**www.maxim-ic.com**

Table 9 shows the pin-outs for the RS-232 interface.

Table 9. RS-232 Serial Interface Pin-Out

Signal Name	Stratix Pin
TIN	M22
ROUT	M23

A/D Converters

The Stratix EP1S25 DSP development board has two 12-bit A/D converters that produce samples at a maximum rate of 125 million-samples per second (MSPS). The A/D subsystem of the board has the following features:

- The data output format from each A/D converter to the Stratix device is in two's complement format.
- The circuit has a wideband, AC-coupled, differential input useful for IF sampling. The analog inputs are transformer-coupled to the A/D converter in order to create a balanced input. To maximize performance, two transformers are used in series. The Analog Devices data sheet for the AD9433 describes the detailed operation of this circuit.
- The converters' analog inputs can be configured as single-ended or differential, with a 0-Ω resistor (R28, R74). The default configuration is single-ended with the resistor installed.
- Any required anti-aliasing filtering can be performed externally.
- If needed, users can purchase in-line SMA filters from a variety of manufacturers, such as Mini-Circuits (**www.minicircuits.com**).

The transformer-coupled AC circuit has a lower 3-dB frequency, of approximately 1 MHz. The A/D converter is recommended for analog bandwidths up to 350 MHz.

The clock signal that drives the A/D converters can originate from the Stratix device, the external clock input, or the on-board 80-MHz oscillator. Jumper JP23 controls which clock is used. Table 10 provides an explanation of how to select these three clock signals. The selected clock will pass through a differential LVPECL buffer before arriving at the clock input to both A/D converters.

Table 10. A/D JP23 Clock Source Settings

JP23 Setting	Clock Source	Signal Name
Pins 1 and 2	On-board 80-MHz oscillator	CLK_OSC
Pins 3 and 4	Stratix pin E15	CLK_OPT_ATOD
Pins 5 and 6	SMA connector JP1	CLK_SMA1_IN

Table 11 lists reference information for the A/D converters.

Table 11. A/D Converter Reference

Item	Description
Board reference	JP6, JP11
Part number	AD9433
Device description	12-bit, 125-MSPS A/D converter
Voltage	3.3-V digital V_{DD}, 5.0-V analog V_{DD}
Manufacturer	Analog Devices
Manufacturer web site	**www.analog.com**

A/D Stratix Pin-Outs

Table 12 and Table 13 show the A/D1 (U10, JP6) and A/D2 (U30, JP11) Stratix pin-outs.

Table 12. A/D1 (U10, JP6) Stratix Pin-Outs

Signal Name	Stratix Pin
ATOD1_b0 (LSB) *(1)*	B5
ATOD1_b1	B6
ATOD1_b2	B7
ATOD1_b3	B8
ATOD1_b4	B9
ATOD1_b5	B10
ATOD1_b6	B11
ATOD1_b7	B12
ATOD1_b8	B13
ATOD1_b9	B16
ATOD1_b10	B17
ATOD1_b11 (MSB) *(2)*	B18

Notes to Table 12:
(1) LSB is least significant bit.
(2) MSB is the most significant bit.

Table 13. A/D2 (U30, JP11) Stratix Pin-Outs	
Signal Name	**Stratix Pin**
ATOD2_b0 (LSB)	D20
ATOD2_b1	D19
ATOD2_b2	C25
ATOD2_b3	C24
ATOD2_b4	C23
ATOD2_b5	C22
ATOD2_b6	C21
ATOD2_b7	C20
ATOD2_b8	C19
ATOD2_b9	C18
ATOD2_b10	B3
ATOD2_b11 (MSB)	B4

D/A Converters

The Stratix EP1S25 DSP development board has two D/A converters. The D/A subsystem of the board has the following features:

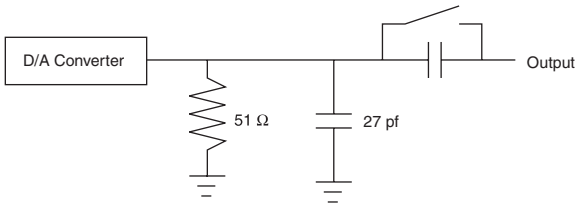
- The converters produce 14-bit samples at a maximum rate of 165 MSPS.
- The analog output from each D/A converter is single-ended.

The D/A converters expect data in an unsigned binary format.

The D/A clock signals are output directly from the Stratix device to the converters.

Figure 5 shows the on-board circuitry after the D/A converter. The output of the D/A converter chip, DAC904, consists of a current source whose maximum value is 20 mA. This output is connected to ground on the board using a 51-Ω resistor, creating a Thevenin equivalent voltage source of 1 V in series with a 51-Ω resistor. When loaded with an external 50-Ω termination, the output swing is reduced to 0.5 V_{PP}. Additionally there is a 27-pF capacitor in parallel with the output resistor resulting in a single-pole, low-pass with an upper 3-dB frequency of approximately 230 MHz when externally loaded. The output is then brought to an SMA connector through a series capacitor, providing a lower 3-dB frequency of approximately 16-KHz when externally loaded. This output capacitor is, by default, bypassed, resulting in a response down to DC. If the jumper is removed, the output is AC-coupled.

Figure 5. On-Board Circuitry after D/A Converter



The DSP kit contains the SLP-50 anti-aliasing filter from Mini-Circuits. This filter provides a 55-MHz cut-off frequency. For systems with other bandwidth requirements, a variety of anti-aliasing filters are available from commercial manufacturers to suit the system requirements.

Table 14 shows the reference information for the anti-aliasing filter. This filter is included with the development but is not connected to the board.

Table 14. Anti-Aliasing Filter Reference

Item	Description
Board reference	N/A
Manufacturer	Mini-circuits
Description	Anti-aliasing filter
Part number	SLP-50
Manufacturer web site	**www.minicircuits.com**

Table 15 lists reference information for the D/A converters.

Table 15. D/A Converter Reference

Item	Description
Board reference	J3, J2
Part number	DAC904
Device description	14-bit, 165-MSPS D/A converter
Voltage	3.3-V digital V_{DD}, 5.0-V analog V_{DD}
Manufacturer	Texas Instruments
Manufacturer web site	**www.ti.com**

D/A Stratix Pin-Outs

Table 16 and Table 17 show the D/A1 (U21, J2) and D/A2 (U23, J3) Stratix pin-outs.

Table 16. D/A1 (U21, J2) Stratix Pin-Outs

Signal Name	Stratix Pin
DTOA1_b13 (MSB)	B19
DTOA1_b12	B20
DTOA1_b11	B21
DTOA1_b10	B22
DTOA1_b9	B23
DTOA1_b8	B24
DTOA1_b7	B25
DTOA1_b6	B26
DTOA1_b5	A26
DTOA1_b4	A25
DTOA1_b3	A24
DTOA1_b2	A23
DTOA1_b1	A22
DTOA1_b0 (LSB)	A21
CLK_DTOA1	AE15

Jumper JP9 is the range select for D/A converter 1. If the jumper is present, the output is DC-coupled. If the jumper is removed, the output is AC-coupled.

Table 17. D/A2 (U23, J3) Stratix Pin-Outs (Part 1 of 2)

Signal Name	Stratix Pin
DTOA2_b13 (MSB) *(1)*	A3
DTOA2_b12	A4
DTOA2_b11	A5
DTOA2_10	A6
DTOA2_b9	A7
DTOA2_b8	A8
DTOA2_b7	A9

Table 17. D/A2 (U23, J3) Stratix Pin-Outs (Part 2 of 2)	
Signal Name	**Stratix Pin**
DTOA2_b6	A10
DTOA2_b5	A11
DTOA2_b4	A13
DTOA2_b3	A16
DTOA2_b2	A18
DTOA2_b1	A19
DTOA2_b0 (LSB)	A20
CLK_DTOA2	AD15

Note to Table 17:
(1) The Texas Instruments (TI) naming conventions differ from those of Altera Corporation. The TI data sheet for the DAC 904 D/A converter lists bit 1 as the MSB and bit 14 as the LSB. For bus naming consistency, this data sheet refers to bit 13 as the MSB, and bit 0 as the LSB.

Jumper JP10 is the range select to D/A converter 2. If the jumper is present, the output is DC-coupled. If the jumper is removed, the output is AC-coupled.

Memory

The Stratix EP1S25 DSP development board has two banks of 7.5-ns synchronous 256 × 36 SRAM, using four 18-bit wide memory chips. The SRAM can be used independently, or combined to have a 36-bit wide organization. To support high data rates and multiple concurrent processing, use the memory as two independent 36-bit wide memory buses.

The second component of the memory subsystem is comprised of a single on-board 32-Mbit flash memory device.

SRAM

Table 18 lists reference information for the SRAM memories.

Table 18. Memory Reference Note (1) (Part 1 of 2)	
Item	**Description**
Board reference	U34, U35, U36, U37
Part number	CY7C1325A
Device description	3.3V, 7.5-ns 128K × 18 SRAM

Table 18. Memory Reference Note (1) (Part 2 of 2)	
Manufacturer	Cypress Semiconductor
Manufacturer web site	**www.cypress.com**

Note to Table 18:
(1) Periodically, SRAM devices from Alliance Corporation or IDT may be used. Both of these devices are pin-to-pin compatible with Cypress Semiconductor SRAM devices. The equivalent Alliance part number is AS7C33256PFS18A-TOC. The equivalent IDT part number is 71V3578.

Table 19 lists the characteristics of the SRAM memories on the board.

Table 19. Memory Characteristics

Type	Address Lines	Data Lines	Memory Organization	Size (MB)
SRAM 1	18	36	256K × 36	1
SRAM 2	18	36	256K × 36	1

SRAM Bank 1

Table 20 lists the pin-outs for SRAM Bank 1.

Table 20. SRAM Bank 1 (U34, U35) (Part 1 of 3)

Signal Name	Stratix Pin
SRAM1_D0	N10
SRAM1_D1	N9
SRAM1_D2	N8
SRAM1_D3	N7
SRAM1_D4	N6
SRAM1_D5	N5
SRAM1_D6	N4
SRAM1_D7	D10
SRAM1_D8	D8
SRAM1_D9	M11
SRAM1_D10	M10
SRAM1_D11	M9
SRAM1_D12	M8
SRAM1_D13	M7

Table 20. SRAM Bank 1 (U34, U35) (Part 2 of 3)

Signal Name	Stratix Pin
SRAM1_D14	M6
SRAM1_D15	M5
SRAM1_D16	M4
SRAM1_D17	D9
SRAM1_D18	D7
SRAM1_D19	L11
SRAM1_D20	L10
SRAM1_D21	L9
SRAM1_D22	L8
SRAM1_D23	L7
SRAM1_D24	L6
SRAM1_D25	K10
SRAM1_D26	L5
SRAM1_D27	L4
SRAM1_D28	L3
SRAM1_D29	C12
SRAM1_D30	D6
SRAM1_D31	K8
SRAM1_D32	K7
SRAM1_D33	K6
SRAM1_D34	K5
SRAM1_D35	K4
SRAM1_A0	H7
SRAM1_A1	H6
SRAM1_A2	H5
SRAM1_A3	H4
SRAM1_A4	H3
SRAM1_A5	C6
SRAM1_A6	C7
SRAM1_A7	G12
SRAM1_A8	G11
SRAM1_A9	G9
SRAM1_A10	G8

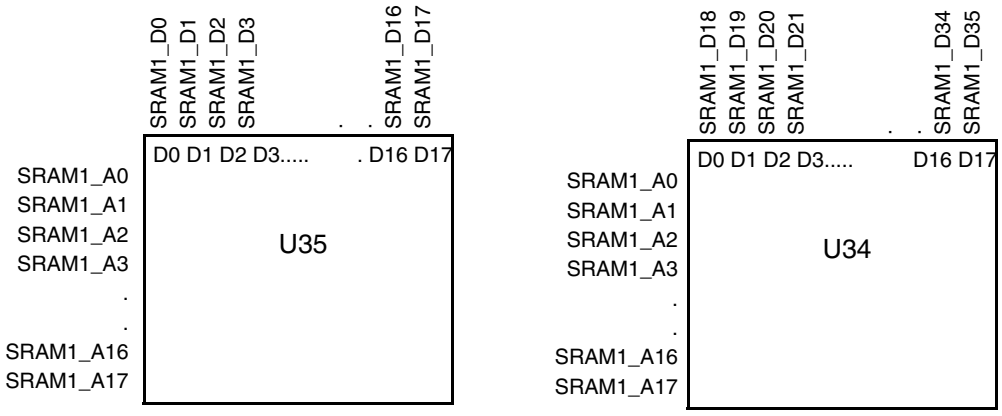
Table 20. SRAM Bank 1 (U34, U35) (Part 3 of 3)

Signal Name	Stratix Pin
SRAM1_A11	G7
SRAM1_A12	G6
SRAM1_A13	G5
SRAM1_A14	G4
SRAM1_A15	G3
SRAM1_A16	C4
SRAM1_A17	C5
SRAM1B_OE_N	T6
SRAM1A_OE_N	T7
SRAM1B_CE_N	T8
SRAM1A_CE_N	T9
SRAM1B_WEL_N	T10
SRAM1A_WEL_N	U10
SRAM1B_BWE_N	U9
SRAM1A_BWE_N	U8
SRAM1B_WEH_N	U7
SRAM1A_WEH_N	U6
Mode	D11
CLK_SRAM1	W14
SRAM1_ADSC_N	T4
SRAM1_ADSP_N	T5
SRAM1_ADV_N	D12

SRAM Bank 1 consists of devices U34 and U35. The control signals for U34 are denoted with an "A," and the control signals for U35 are denoted with a "B." For example, SRAM1A_OE_n is the output enable for U34, and SRAM1B_OE_n is the output enable for U35.

As shown in Figure 6, data bits [17..0] are on U35, and data bits [35..18] are on U34. All address lines are shared.

Figure 6. SRAM1 Data Bits on U34 & U35



SRAM Bank 2

Table 21 lists the pin-outs for SRAM bank 2.

Table 21. SRAM Bank 2 Pin-Outs (U36, U37) (Part 1 of 3)

Signal Name	Stratix Pin
SRAM2_D0	U5
SRAM2_D1	U4
SRAM2_D2	D16
SRAM2_D3	D17
SRAM2_D4	V10
SRAM2_D5	V9
SRAM2_D6	V8
SRAM2_D7	V7
SRAM2_D8	V6
SRAM2_D9	V5
SRAM2_D10	V4
SRAM2_D11	V3
SRAM2_D12	D18
SRAM2_D13	D5

Table 21. SRAM Bank 2 Pin-Outs (U36, U37) (Part 2 of 3)

Signal Name	Stratix Pin
SRAM2_D14	W8
SRAM2_D15	W7
SRAM2_D16	W6
SRAM2_D17	W5
SRAM2_D18	W4
SRAM2_D19	W3
SRAM2_D20	C16
SRAM2_D21	C13
SRAM2_D22	Y11
SRAM2_D23	Y10
SRAM2_D24	Y9
SRAM2_D25	Y8
SRAM2_D26	Y7
SRAM2_D27	Y6
SRAM2_D28	Y5
SRAM2_D29	Y4
SRAM2_D30	Y3
SRAM2_D31	E6
SRAM2_D32	C17
SRAM2_D33	E10
SRAM2_D34	E8
SRAM2_D35	D13
SRAM2_A0	K3
SRAM2_A1	C10
SRAM2_A2	C11
SRAM2_A3	J11
SRAM2_A4	J10
SRAM2_A5	J9
SRAM2_A6	J8
SRAM2_A7	J7
SRAM2_A8	J6
SRAM2_A9	J5
SRAM2_A10	J4
SRAM2_A11	J3

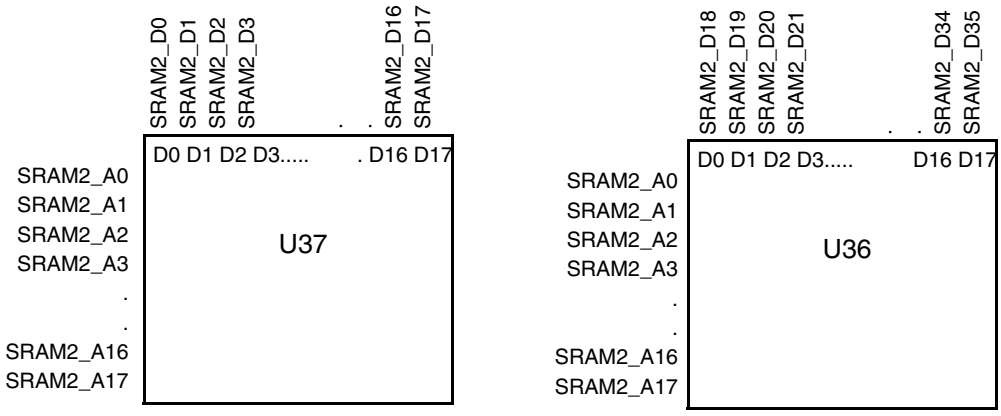
Table 21. SRAM Bank 2 Pin-Outs (U36, U37) (Part 3 of 3)

Signal Name	Stratix Pin
SRAM2_A12	C8
SRAM2_A13	C9
SRAM2_A14	H11
SRAM2_A15	H10
SRAM2_A16	H9
SRAM2_A17	H8
SRAM2D_OE_N	K21
SRAM2C_OE_N	K22
SRAM2D_CE_N	K23
SRAM2C_CE_N	K24
SRAM2D_WEL_N	K25
SRAM2C_WEL_N	K26
SRAM2D_BWE_N	D23
SRAM2C_BWE_N	D21
SRAM2D_WEH_N	J26
SRAM2C_WEH_N	J25
Mode	D11
CLK_SRAM2	W15
SRAM2_ADSC_N	F11
SRAM2_ADSP_N	K19
SRAM2_ADV_N	AB11

SRAM Bank 2 consists of chips U36 and U37. The control signals for U36 are denoted with a "C," and the control signals for U37 are denoted with a "D." For example, SRAM1C_OE_n is the output enable for U36, and SRAM1D_OE_n is the output enable for U37.

As shown in Figure 7, data bits [17..0] are on U37, and data bits [35..18] are on U36. All address lines are shared.

Figure 7. SRAM2 Data Bits on U36 & U37



Flash Device Description

The specifications and pin-outs for the 32-Mbit flash memory device on the Stratix EP1S25 DSP development board are given in this section.

Table 22 gives details on the specifications and manufacturer for the flash memory device.

Table 22. Flash Memory Device Reference

Feature	Flash Memory
Board reference	U3
Part number	AM29LV320DT
Device description	32 Mbit flash memory
Voltage	3.3-V
Manufacturer	AMD
Manufacturer web site	**www.amd.com**

Flash Pin-Outs

Table 23 lists pin-outs for the flash memory device.

Table 23. Flash Pin-Outs (Part 1 of 2)

Signal Name	Stratix Pin
Flash_addr1	AG25
Flash_addr2	H19
Flash_addr3	AD10
Flash_addr4	AH25
Flash_addr5	AH24
Flash_addr6	AH23
Flash_addr7	AH22
Flash_addr8	AH21
Flash_addr9	AH20
Flash_addr10	AH19
Flash_addr11	AH16
Flash_addr12	AH13
Flash_addr13	AH11
Flash_addr14	AH10
Flash_addr15	AH9
Flash_addr16	AH8
Flash_addr17	AH7
Flash_addr18	AH6
Flash_addr19	AH5
Flash_addr20	AH4
Flash_addr21 *(1)*	AH3
Flash_data0	AG24, H12
Flash_data1	F12
Flash_data2	J12
Flash_data3	M12
Flash_data4	H17
Flash_data5	K18
Flash_data6	H18
Flash_data7	G18
Flash_data8	AG23
Flash_data9	AG22

Table 23. Flash Pin-Outs (Part 2 of 2)

Signal Name	Stratix Pin
Flash_data10	AG21
Flash_data11	AG20
Flash_data12	AG19
Flash_data13	AG18
Flash_data14	AG17
Flash_data15 *(2)*	AG16
Flash_R/W_n	D22
Flash_reset	AD13
Flash_WP_ACC_n	AD12
Flash_rdy/bsy_n	T26
Flash_byte_n	F23
Flash_OE_n	F5

Notes to Table 23:

(1) Flash address 21 is connected to jumper JP18. If this jumper is in place, signal Flash_addr21 is pulled down to GND. If the connector is removed, Flash_addr21 is pulled up to V_{CCIO}. Stratix pin AH3 can over-power the pull-up or pull-down.

(2) Flash_data15 doubles as flash address bit 0 when the flash is in byte mode.

Debugging Interfaces

The Stratix EP1S25 DSP development board has the following two interfaces to allow users to debug their designs:

- Two Mictor-type connectors to support Agilent logic analyzers
- 90 digital I/O signals, available on the 0.1-inch headers, and connected directly to the Stratix device

Logic Analyzer Interface (Mictor Connectors)

The Stratix EP1S25 DSP development board has two Mictor-type connectors to support Agilent logic analyzers, or a high-speed off-board solution.

Mictor Connector A

Table 24 gives the pin-outs for Mictor connector A.

Table 24. Mictor Connector A (J9) Stratix Pin-Outs (Part 1 of 2)

Signal Name	Stratix Pin
DEBUG_A0	Y19
DEBUG_A1	Y20
DEBUG_A2	Y21
DEBUG_A3	Y22
DEBUG_A4	Y23
DEBUG_A5	Y24
DEBUG_A6	Y25
DEBUG_A7	Y26
DEBUG_A8	E21
DEBUG_A9	E23
DEBUG_A10	AA3
DEBUG_A11	AA4
DEBUG_A12	AA5
DEBUG_A13	AA6
DEBUG_A14	AA7
DEBUG_A15	AA8
DEBUG_A16	AA9
DEBUG_A17	AA10
DEBUG_A18	AA11
DEBUG_A19	AA20

Table 24. Mictor Connector A (J9) Stratix Pin-Outs (Part 2 of 2)	
Signal Name	**Stratix Pin**
DEBUG_A20	AA21
DEBUG_A21	AA22
DEBUG_A22	AA23
DEBUG_A23	AA24
DEBUG_A24	AA25
DEBUG_A25	AA26
DEBUG_A26	G25
DEBUG_A27	G26
DEBUG_A28	G24
DEBUG_A29	G23
DEBUG_A30	AB26
DEBUG_A31	AB25
CLK_DEBUGA	Y16

Mictor Connector B

Table 25 gives the pin-outs for Mictor connector B.

Table 25. Mictor Connector B (J10) Stratix Pin-Outs (Part 1 of 2)	
Signal Name	**Stratix Pin**
DEBUG_B0	AF11
DEBUG_B1	AF12
DEBUG_B2	AF13
DEBUG_B3	AF16
DEBUG_B4	AF17
DEBUG_B5	AF18
DEBUG_B6	AF19
DEBUG_B7	AF20
DEBUG_B8	AF21
DEBUG_B9	AF22
DEBUG_B10	AF23
DEBUG_B11	AF24
DEBUG_B12	H20

Table 25. Mictor Connector B (J10) Stratix Pin-Outs (Part 2 of 2)

Signal Name	Stratix Pin
DEBUG_B13	H21
DEBUG_B14	H24
DEBUG_B15	H26
DEBUG_B16	H23
DEBUG_B17	H22
DEBUG_B18	AE24
DEBUG_B19	AE23
DEBUG_B20	AE22
DEBUG_B21	AE21
DEBUG_B22	AE20
DEBUG_B23	AE19
DEBUG_B24	AE18
DEBUG_B25	AE17
DEBUG_B26	AE16
DEBUG_B27	AE13
DEBUG_B28	AE12
DEBUG_B29	AE11
DEBUG_B30	AE10
DEBUG_B31	AD16
CLK_DEBUGB	K16

0.1-Inch Digital I/O Headers

The board has a total of 90 digital I/O signals, available on the 0.1-inch headers, and connected directly to the Stratix device. Additionally, the connectors contain ground signals to ensure the integrity of the signals, and to provide for the Analog Devices external A/D connectors.

JP7 and JP8 are a matched pair of right-angle connectors, which allow the user to join two DSP boards by connecting the JP7 connector on one board to the JP8 connector on the second.

The Stratix pins connected to JP19 and J22 are also connected to JP7. Similarly, the Stratix pins which drive JP8 also drive JP20, JP21, and JP24. See Table 26 and Table 27 for details on which Stratix pins are connected to both places.

When connecting these pins to external circuitry, the user must adhere to the voltage restrictions specified in the *Stratix Programmable Logic Device Family Data Sheet*. Specifically, the I/O pins are not 5.0-V tolerant and should not be directly connected to logic powered from a 5.0-V supply.

Digital I/O Headers (JP7, JP19, JP22)

Table 26 shows the pin-outs for the digital I/O headers JP7, JP19, and JP22.

Table 26. Digital I/O Headers (JP7, JP19, JP22) (Part 1 of 2)

Signal Name	Stratix Pin	JP7	JP19	JP22
EVALIO_IN0	C2	1	3	-
EVALIO_IN1	C1	2	5	-
EVALIO_IN2	D2	3	7	-
EVALIO_IN3	D1	5	9	-
EVALIO_IN4	E2	6	11	-
EVALIO_IN5	E1	7	13	-
EVALIO_IN6	F2	9	15	-
EVALIO_IN7	F1	10	17	-
EVALIO_IN8	G2	11	19	-
EVALIO_IN9	G1	13	21	-
EVALIO_IN10	H2	14	23	-
EVALIO_IN11	H1	15	25	-
EVALIO_IN12	J2	17	27	-
EVALIO_IN13	J1	18	29	-
EVALIO_IN14	K2	19	31	-
EVALIO_IN15	K1	21	33	-
EVALIO_IN16	L2	22	37	-
EVALIO_IN17	L1	23	-	3
EVALIO_IN18	M2	25	-	5
EVALIO_IN19	N1	26	-	7
EVALIO_IN20	M3	27	-	9

Table 26. Digital I/O Headers (JP7, JP19, JP22) (Part 2 of 2)				
Signal Name	**Stratix Pin**	**JP7**	**JP19**	**JP22**
EVALIO_IN21	N3	29	-	11
EVALIO_IN22	T1	30	-	13
EVALIO_IN23	T3	31	-	15
EVALIO_IN24	U2	33	-	17
EVALIO_IN25	U3	34	-	19
EVALIO_IN26	V1	35	-	21
EVALIO_IN27	V2	37	-	23
EVALIO_IN28	W1	38	-	25
EVALIO_IN29	W2	39	-	27
EVALIO_IN30	Y1	41	-	29
EVALIO_IN31	Y2	42	-	31
EVALIO_IN32	AA1	43	-	33
EVALIO_IN33	AA2	45	-	37
EVALIO_IN34	AB1	46	-	-
EVALIO_IN35	AB2	47	-	-
EVALIO_IN36	AC1	49	-	-
EVALIO_IN37	AC2	50	-	-
EVALIO_IN38	AD1	51	-	-
EVALIO_IN39	AD2	53	-	-
EVALIO_IN40	AE1	54	-	-
EVALIO_IN41	AE2	55	-	-
EVALIO_IN42	AF1	57	-	-
EVALIO_IN43	AF2	58	-	-
CLK_EVALIO_IN44	P25 (CLK1p)	59	-	-

Digital I/O Headers (JP20, JP21, JP24, JP8)

Table 27 lists the pin-outs for digital I/O headers JP20, JP21, JP24, and JP8.

Table 27. Digital I/O Headers (JP20, JP21, JP24, JP8) (Part 1 of 3)					
Signal Name	**Stratix Pin**	**JP20**	**JP21**	**JP24**	**JP8**
EVALIO_OUT0	C27	-	-	3	1
EVALIO_OUT1	C28	-	-	4	2
EVALIO_OUT2	D27	-	-	5	3

Table 27. Digital I/O Headers (JP20, JP21, JP24, JP8) (Part 2 of 3)

Signal Name	Stratix Pin	JP20	JP21	JP24	JP8
EVALIO_OUT3	D28	-	-	6	5
EVALIO_OUT4	E27	-	-	7	6
EVALIO_OUT5	E28	-	-	8	7
EVALIO_OUT6	F27	-	-	9	9
EVALIO_OUT7	F28	-	-	10	10
EVALIO_OUT8	G27	-	-	11	11
EVALIO_OUT9	G28	-	-	12	13
EVALIO_OUT10	H27	-	-	13	14
EVALIO_OUT11	H28	-	-	14	15
EVALIO_OUT12	J27	-	-	15	17
EVALIO_OUT13	J28	-	-	16	18
EVALIO_OUT14	K27	-	-	17	19
EVALIO_OUT15	K28	-	-	18	21
EVALIO_OUT16	L27	-	-	21	22
EVALIO_OUT17	L28	-	-	23	23
EVALIO_OUT18	M27	-	-	25	25
EVALIO_OUT19	N28	-	-	27	26
EVALIO_OUT20	T28	-	-	28	27
EVALIO_OUT21	U27	-	-	29	29
EVALIO_OUT22	V28	-	-	31	30
EVALIO_OUT23	V27	-	-	32	31
EVALIO_OUT24	W28	-	-	33	33
EVALIO_OUT25	W27	-	-	35	34
EVALIO_OUT26	Y28	-	-	36	35
EVALIO_OUT27	Y27	-	-	37	37
EVALIO_OUT28	AA28	-	-	39	38
EVALIO_OUT29	AA27	4	-	-	39
EVALIO_OUT30	AB28	5	-	-	41
EVALIO_OUT31	AB27	6	-	-	42
EVALIO_OUT32	AC28	7	-	-	43
EVALIO_OUT33	AC27	8	-	-	45
EVALIO_OUT34	AD28	9	-	-	46
EVALIO_OUT35	AD27	10	-	-	47
EVALIO_OUT36	AE28	11	-	-	49

Table 27. Digital I/O Headers (JP20, JP21, JP24, JP8) (Part 3 of 3)

Signal Name	Stratix Pin	JP20	JP21	JP24	JP8
EVALIO_OUT37	AD24	12	-	-	50
EVALIO_OUT38	AF28	13	-	-	51
EVALIO_OUT39	AE27	14	-	-	53
EVALIO_OUT40	AE25	-	-	-	54
EVALIO_OUT41	AF27	-	-	-	55
EVALIO_OUT42	AF25	-	9	-	57
EVALIO_OUT43	AG26	-	11	-	58
CLK_EVALIO_OUT44	W16 (pll6out3p)	-	13	-	59

Expansion Interfaces

There are five ways in which the Stratix EP1S25 DSP development board was designed to interface with other boards and devices. The board is equipped with the following interfaces:

- A TI-EVM, located on the underside of the board (J11, J12)
- A Front Panel Data Port (FPDP) Footprint (J4)
- Two 0.1-inch headers specifically designed to be used with external analog-to-digital devices made by Analog Devices Corporation (JP19, JP22)
- An Altera expansion prototype connector
- A breadboard/prototype area that allows for the connection of custom components

TI-EVM

The TI-EVM is specifically designed to work with TI boards that have the EVM interface. See the Texas Instruments web site for details on which of their boards feature this connector.

A portion of the Stratix pins routed to the TI-EVM connector (J11, J12) are also routed to the four rows of through-holes, labeled J4. These four rows of pins comprise a footprint for an FPDP, which can be added to the board.

TI-EVM Connector / FPDP Connector

Table 28 lists the pin-outs for the TI-EVM and FPDP connectors.

Table 28. TI-EVM Connector (J11, J12) / FPDP Connector (J4) (Part 1 of 3)

TI-EVM Signal Name	FPDP Signal Name	Stratix Pin
J11		
TI_CLKX0	-	G22
TI_FSX0	-	G21
TI_CLKR0	-	AC24
TI_FSR0	-	AC23
TI_STAT0	-	AE8
TI_DRO	-	AE4
CLK_TI_OUT2	-	P27
TI_DMAC0	-	AE9
TI_CNTL0	-	AE7
TI_INUM0	-	AE6
TI_IACK	-	AE5
TI_DX0	-	F7
J12		
TI_ARDY	-	AD8
TI_CE1_N	-	F4
TI_AOE_N	-	AD6
TI_AWE_N	-	AD5
TI_ARE_N	-	AD23
TI_A2	-	AF10
TI_A3	-	AF9
TI_A4	-	AF8
TI_A5	-	AF7
TI_A6	-	AF6
TI_A7	-	AF5
TI_A8	-	AF4
TI_A9	-	F9
TI_A10	-	F8
TI_A11	-	AG3
TI_A12	-	AG4
TI_A13	-	AG5

Table 28. TI-EVM Connector (J11, J12) / FPDP Connector (J4) (Part 2 of 3)

TI-EVM Signal Name	FPDP Signal Name	Stratix Pin
TI_A14	-	AG6
TI_A15	-	AG7
TI_A16	-	AG8
TI_A17	-	AG9
TI_A18	-	AG10
TI_A19	-	AG11
TI_A20	-	AG12
TI_A21	-	AG13
TI_BE_N0	-	AD17
TI_BE_N1	-	AD18
TI_BE_N2	-	AD19
TI_BE_N3	-	AD21
TI_D0	FPDP_D0	U20
TI_D1	FPDP_D1	U21
TI_D2	FPDP_D2	U22
TI_D3	FPDP_D3	U23
TI_D4	FPDP_D4	U24
TI_D5	FPDP_D5	U25
TI_D6	FPDP_D6	U26
TI_D7	FPDP_D7	F22
TI_D8	FPDP_D8	V11
TI_D9	FPDP_D9	V18
TI_D10	FPDP_D10	V19
TI_D11	FPDP_D11	V20
TI_D12	FPDP_D12	V21
TI_D13	FPDP_D13	V22
TI_D14	FPDP_D14	V23
TI_D15	FPDP_D15	V24
TI_D16	FPDP_D16	V25
TI_D17	FPDP_D17	V26
TI_D18	FPDP_D18	F20
TI_D19	FPDP_D19	F21
TI_D20	FPDP_D20	W10
TI_D21	FPDP_D21	W12

Table 28. TI-EVM Connector (J11, J12) / FPDP Connector (J4) (Part 3 of 3)

TI-EVM Signal Name	FPDP Signal Name	Stratix Pin
TI_D22	FPDP_D22	W18
TI_D23	FPDP_D23	W19
TI_D24	FPDP_D24	W21
TI_D25	FPDP_D25	W22
TI_D26	FPDP_D26	W23
TI_D27	FPDP_D27	W24
TI_D28	FPDP_D28	W25
TI_D29	FPDP_D29	W26
TI_D30	FPDP_D30	F17
TI_D31	FPDP_D31	F18
-	FPDP_STROB	T19
-	FPDP_NRDY_N	T20
-	FPDP_DIR_N	T21
-	FPDP_SUSPEND_N	T22
-	FPDP_P102	T23
-	FPDP_P101	T24
-	FPDP_STORBEN	AG15
-	FPDP_PSTROBE	AF15
-	FPDP_DVALID_N	U19
-	FPDP_SYNC_N	T25

Analog Devices Corporation External A/D Support

The Stratix EP1S25 DSP development board supports Analog Devices A/D converters via two 40-pin 0.1-inch digital I/O headers (JP19, JP22). The Analog Devices converters also require a clock, which can be sourced from the CLK_SMAOUT1 (JP2) or CLK_SMAOUT2 (JP4) external clock outputs. These two dual-purpose digital I/O headers can support a maximum of the following three converters.

- Two AD9433 converters
- Two AD6645 converters
- One AD9430 converter

The Stratix pins connected to JP19 and J22 are also connected to JP7. Similarly, the Stratix pins that drive JP8 also drive JP20, JP21, and JP24. See Table 26 on page 36 and Table 27 on page 37 for details on which Stratix pins are connected to both places.

Altera Expansion Prototype Connector

Headers JP20, JP21, and JP24 collectively form a standard-footprint, mechanically-stable connection that may be used, for example, as an interface to a special-function daughter card.

Contact your Altera sales representative for a list of available expansion daughter cards that can be used with the Stratix EP1S25 DSP development board.

The 3.3-V expansion prototype connector interface includes the following.

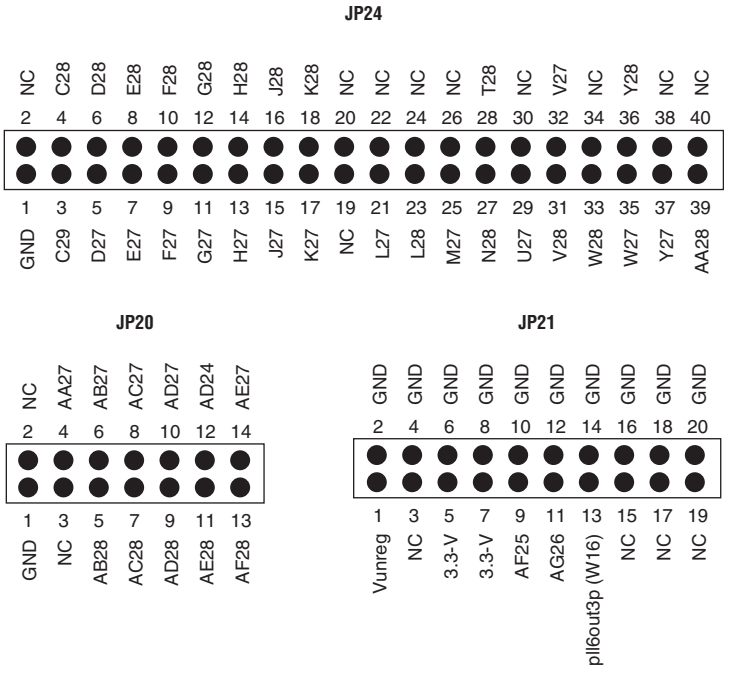
- 40 Stratix device general-purpose I/O signals
- A Stratix device clock-input (for daughter cards that drive a clock to the programmable logic device)
- Two regulated 3.3-V power-supply pins (500 mA total maximum load)
- An unregulated power-supply pin (connects directly to the J1 power-input plug)
- Numerous ground connections

The Stratix pins that drive JP8 also drive JP20, JP21, and JP24. See Table 26 on page 36 and Table 27 on page 37 for details on which Stratix pins are connected to both places.

JP20, JP21, JP24 Connector Pin-Outs

Figure 8 shows the relative orientation of the connectors and pins for JP20, JP21, and JP24.

Figure 8. Pin-Outs for Headers JP20, JP21, JP24



Prototyping Area

The prototyping area of the board provides room for adding user-selected electronic components. This area is a grid of plated through--holes on 0.1-inch centers. Thirty Stratix I/O pins are connected to the inside column (the column closest to the middle of the board) of pins in the grid. These pins, and each column, are labeled on the board for easy identification. As shown in Table 29, one column of ground pins and one column of 3.3 V V_{CCIO} pins provide power to the grid. The remaining columns (labeled 2, 3, 6, 7, and 8 on the board) are not connected to any power or pins, and are available for the addition of custom components.

Table 29 shows the column functions in the prototyping area of the board.

Table 29. Column Functions in the Prototyping Area

Column	Function
1	Stratix pins (see Table 30)
2	Unconnected
3	Unconnected
4	V_{CCIO} (3.3 V)
5	GND
6	Unconnected
7	Unconnected
8	Unconnected

Prototyping Area Pin-Out

Table 30 shows the pin-outs for the prototyping area of the Stratix EP1S25 DSP development board.

Table 30. Prototyping Area Pin-Outs (Part 1 of 2)

Signal Name	Stratix Pin
PROTO1	J24
PROTO2	J23
PROTO3	J22
PROTO4	J21
PROTO5	J20
PROTO6	J18
PROTO7	AC22
PROTO8	AC20
PROTO9	AC10
PROTO10	AC7
PROTO11	AC6
PROTO12	AC5
PROTO13	F3
PROTO14	E13
PROTO15	AB23
PROTO16	AB24
PROTO17	AB22

Table 30. Prototyping Area Pin-Outs (Part 2 of 2)	
Signal Name	**Stratix Pin**
PROTO18	AB21
PROTO19	AB20
PROTO20	AB19
PROTO21	AB18
PROTO22	AB9
PROTO23	AB8
PROTO24	AB7
PROTO25	AB6
PROTO26	AB5
PROTO27	AB4
PROTO28	AB3
PROTO29	E12
PROTO30	AH26

Jumper Settings

Table 31 summarizes the jumper settings for the Stratix EP1S25 DSP development board.

Table 31. Jumper Settings			
Number	**Function**	**Setting**	**Selected Option**
JP9	D/A1 AC/DC coupling select	Not Jumpered	AC Coupled
		Jumpered	DC Coupled
JP10	D/A2 AC/DC coupling select	Not Jumpered	AC Coupled
		Jumpered	DC Coupled
JP23	A/D clock select	1 and 2	80-MHz Oscillator
		3 and 4	Stratix Pin E15
		5 and 6	External Clock
JP18 (by C48)	Flash top/bottom select	Not Jumpered	Flash Address Pin 21 = VCC
		Jumpered	Flash Address Pin 21 = GND

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